

General Description

The WST3392 is the highest performance trench Dual N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the small power switching and load switch applications.

The WST3392 meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

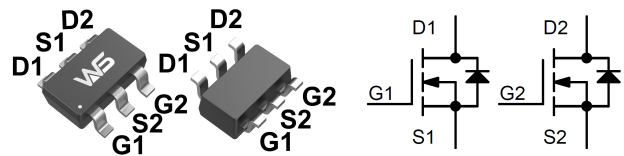
Product Summary

BVDSS	RDSON	ID
30V	40mΩ	3.7A

Applications

- Power management in portable and battery operated products
- One cell battery pack protection

SOT-23-6L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	3.7	A
$I_D@T_C=70^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	3.0	A
I_{DM}	Pulsed Drain Current ²	20	A
$P_D@T_A=25^\circ C$	Total Power Dissipation ³	1.15	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	---	110	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	80	$^\circ C/W$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.028	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =3.5A	---	40	50	mΩ
		V _{GS} =6V, I _D =2A	---	45	65	
		V _{GS} =4.5V, I _D =2A	---	58	73	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.0	1.5	2.0	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-3.21	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =30V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =30V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =5A	---	12	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	4	6	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =15V, V _{GS} =10V, I _D =3.5A	---	4.05	5	nC
Q _{gs}	Gate-Source Charge		---	0.55	0.8	
Q _{gd}	Gate-Drain Charge		---	1.0	1.8	
T _{d(on)}	Turn-On Delay Time	V _{DD} =15V, V _{GEN} =10V, R _G =3Ω I _D =1.0A, R _L =4.2Ω.	---	4.5	---	ns
T _r	Rise Time		---	1.5	---	
T _{d(off)}	Turn-Off Delay Time		---	18.5	---	
T _f	Fall Time		---	15.5	---	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	170	210	pF
C _{oss}	Output Capacitance		---	35	45	
C _{rss}	Reverse Transfer Capacitance		---	23	30	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	1.5	A
I _{SM}	Pulsed Source Current ^{2,4}		---	---	3.5	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _{SD} =3.5A, T _J =25°C	---	---	1.0	V
t _{rr}	Reverse Recovery Time	I _F =3.5A, dI/dt=100A/μs, T _J =25°C	---	7.5	---	nS
Q _{rr}	Reverse Recovery Charge		---	2.5	---	nC

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
3. The power dissipation is limited by 150°C junction temperature
4. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

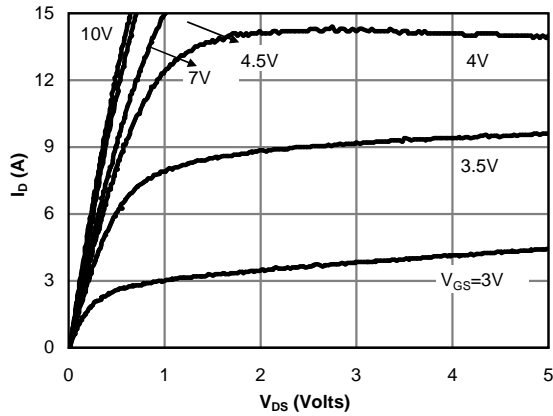


Figure 1: On-Region Characteristics (Note E)

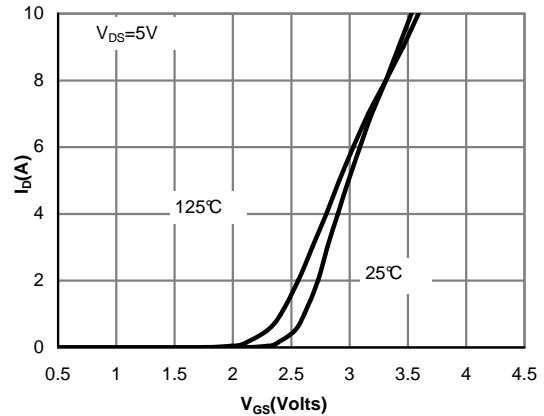


Figure 2: Transfer Characteristics (Note E)

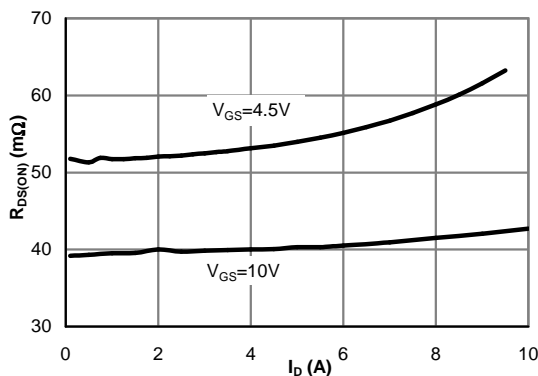


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

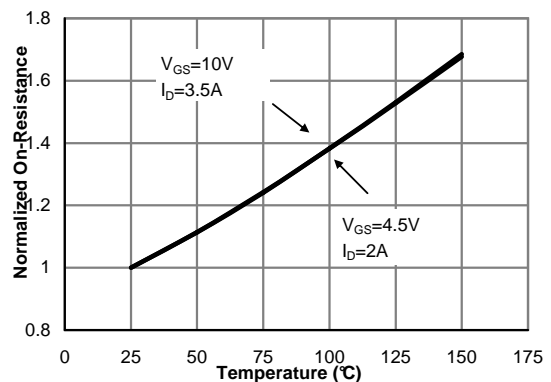


Figure 4: On-Resistance vs. Junction Temperature (Note E)

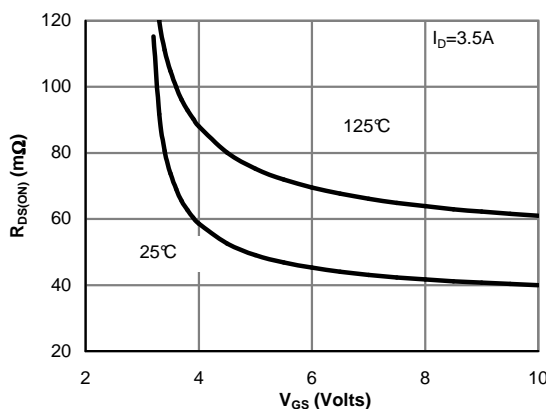


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

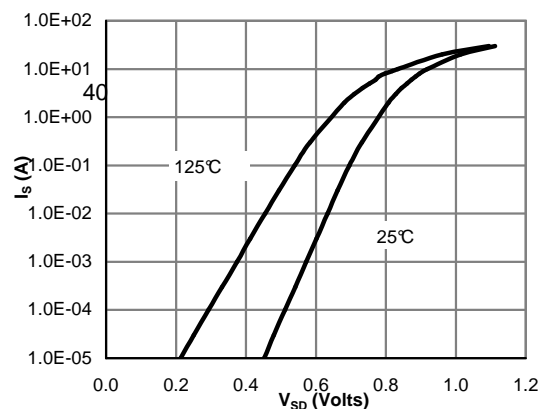


Figure 6: Body-Diode Characteristics (Note E)

Typical Characteristics

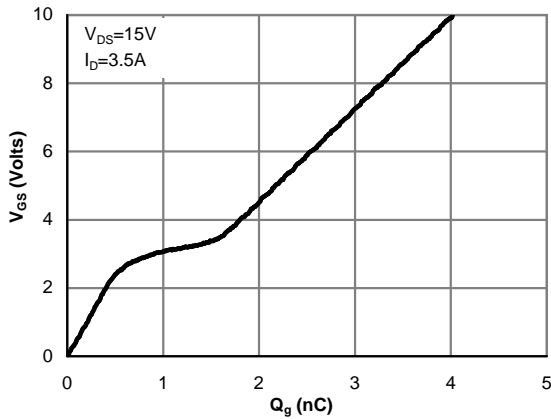


Figure 7: Gate-Charge Characteristics

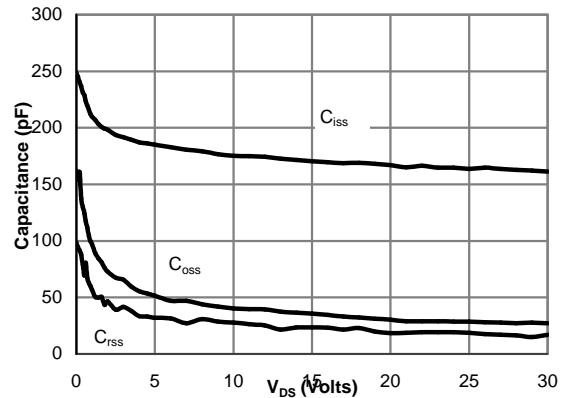


Figure 8: Capacitance Characteristics

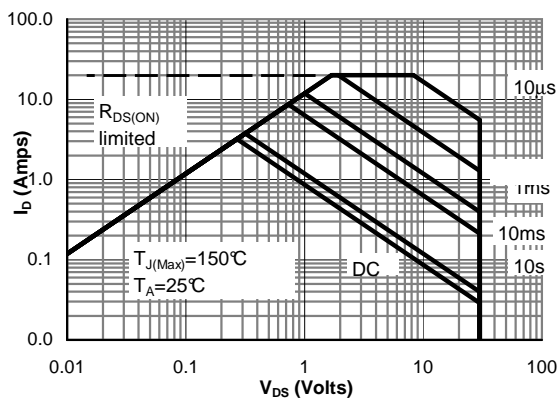


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

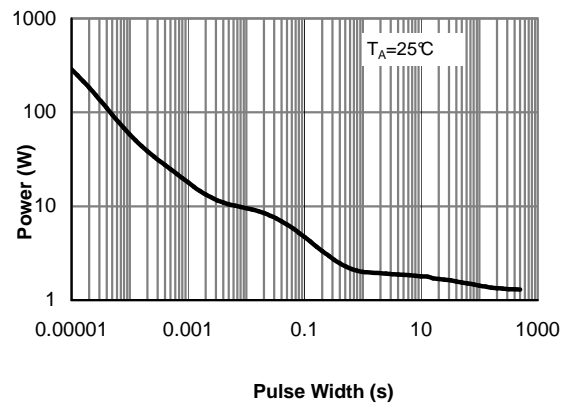


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

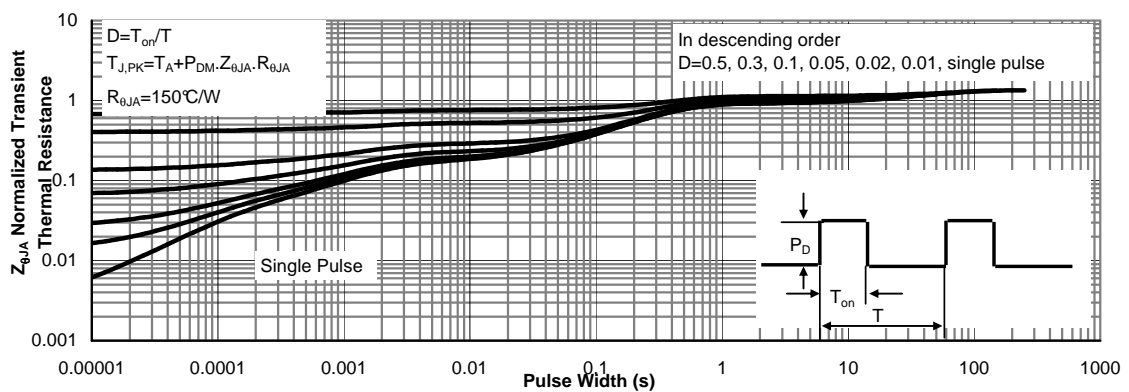


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



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