

General Description

The WSD6034DN33 is the highest performance trench N-Ch and P-Channel MOSFET with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications .

The WSD6034DN33 meet the RoHS and Green Product requirement, 100% E_{AS} guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

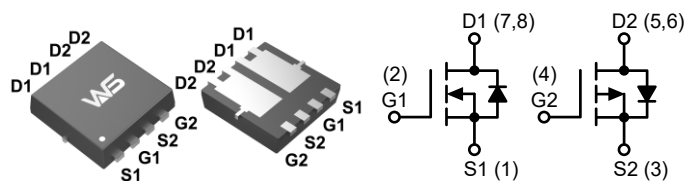
Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D
60V	35mΩ	15A
-60V	80mΩ	-10A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter.
- Networking DC-DC Power System
- Load Switch

DFN3X3-8L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	60	-60	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	15	-10	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	6	-4	A
I_{DM}	Pulsed Drain Current ²	45	-30	A
EAS	Single Pulse Avalanche Energy ³	16	18	mJ
I_{AS}	Avalanche Current	8	-9	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	13.3	13.3	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	85	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	50	$^\circ C/W$

N-Channel Electrical Characteristics ($T_A=25^{\circ}\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	60	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.063	---	$\text{V}/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V$, $I_D=5A$	---	35	40	$\text{m}\Omega$
		$V_{GS}=4.5V$, $I_D=3A$	---	40	48	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.0	2.0	3.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.24	---	$\text{mV}/^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=48V$, $V_{GS}=0V$, $T_J=25^{\circ}\text{C}$	---	---	1	μA
		$V_{DS}=48V$, $V_{GS}=0V$, $T_J=85^{\circ}\text{C}$	---	---	30	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V$, $I_D=5A$	---	21	---	S
R_g	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	3.0	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=30V$, $V_{GS}=10V$, $I_D=5A$	---	4.3	---	nC
Q_{gs}	Gate-Source Charge		---	1.6	---	
Q_{gd}	Gate-Drain Charge		---	1.5	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V$, $V_{GS}=10V$, $R_G=6\Omega$, $I_D=1A$	---	7	13	ns
T_r	Rise Time		---	7	13	
$T_{d(off)}$	Turn-Off Delay Time		---	5	9	
T_f	Fall Time		---	18	33	
C_{iss}	Input Capacitance	$V_{DS}=15V$, $V_{GS}=0V$, $f=1\text{MHz}$	---	400	520	pF
C_{oss}	Output Capacitance		---	43	---	
C_{rss}	Reverse Transfer Capacitance		---	24	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	---	---	15	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	45	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V$, $I_S=1.7A$, $T_J=25^{\circ}\text{C}$	---	0.8	1.3	V

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper, $t<10\text{sec}$.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V$, $V_{GS}=10V$, $L=0.5\text{mH}$, $I_{AS}=8A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Channel Electrical Characteristics ($T_A=25^{\circ}\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-60	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.03	---	$\text{V}/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-3.5A$	---	80	93	$\text{m}\Omega$
		$V_{GS}=-4.5V, I_D=-2.1A$	---	100	128	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	-2.0	-3.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4.56	---	$\text{mV}/^{\circ}\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-48V, V_{GS}=0V, T_J=25^{\circ}\text{C}$	---	---	-1	μA
		$V_{DS}=-48V, V_{GS}=0V, T_J=85^{\circ}\text{C}$	---	---	-30	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=-5V, I_D=-4.5A$	---	15	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	11	---	Ω
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-30V, V_{GS}=-10V, I_D=-3.5A$	---	5.2	---	nC
Q_{gs}	Gate-Source Charge		---	1.9	---	
Q_{gd}	Gate-Drain Charge		---	2.1	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-30V, V_{GS}=-10V, R_G=6\Omega, I_D=-1A,$	---	4	7	ns
T_r	Rise Time		---	8	14	
$T_{d(off)}$	Turn-Off Delay Time		---	22	40	
T_f	Fall Time		---	39	70	
C_{iss}	Input Capacitance	$V_{DS}=-30V, V_{GS}=0V, f=1\text{MHz}$	---	455	592	pF
C_{oss}	Output Capacitance		---	51	---	
C_{rss}	Reverse Transfer Capacitance		---	32	---	

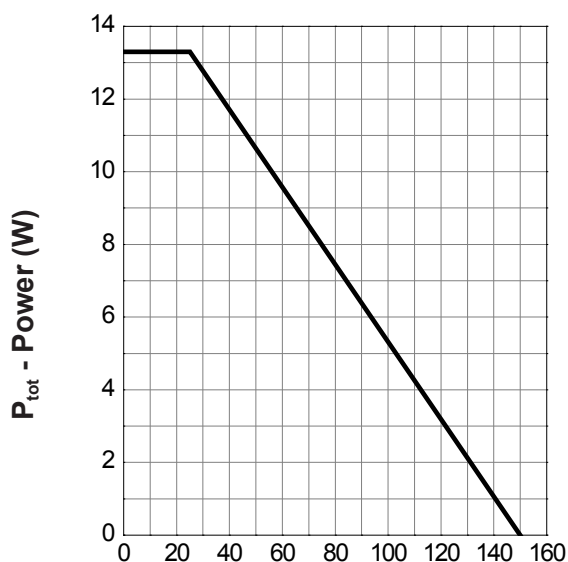
Diode Characteristics

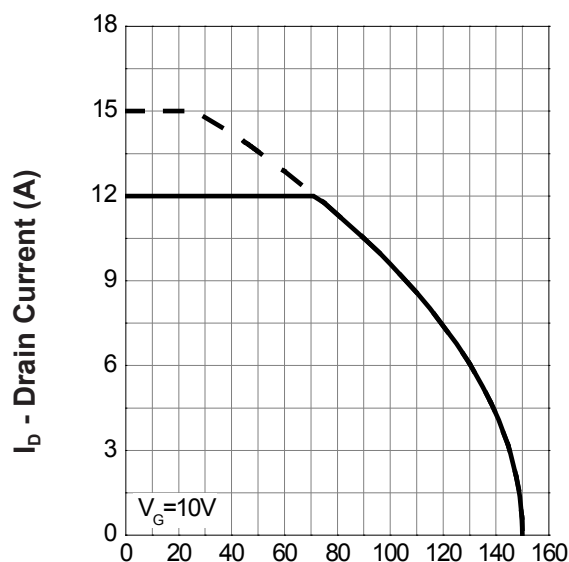
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,6}	$V_G=V_D=0V$, Force Current	---	---	-15	A
I_{SM}	Pulsed Source Current ^{2,6}		---	---	-50	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1.5A, T_J=25^{\circ}\text{C}$	---	-0.8	-1.0	V

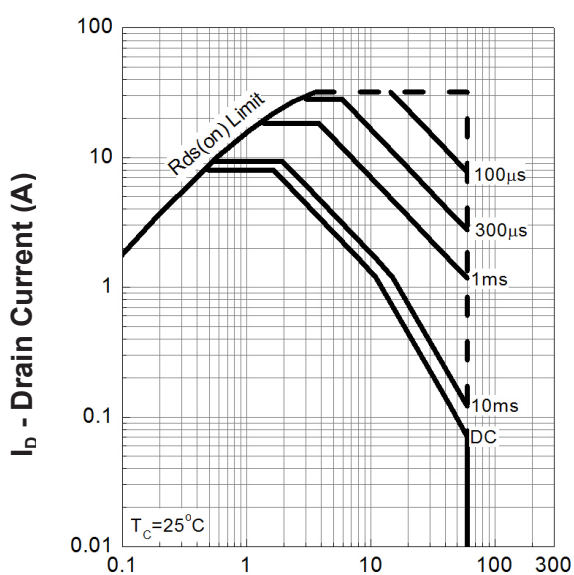
Note :

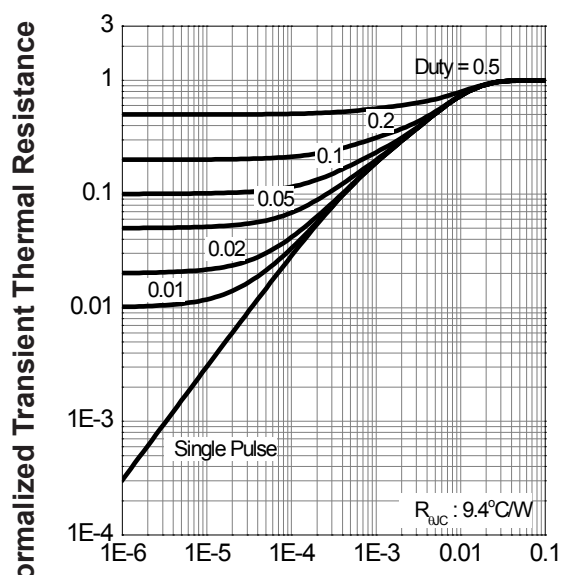
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- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=-25V, V_{GS}=-10V, L=0.5\text{mH}, I_{AS}=-9A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

Power Dissipation

 T_c - Case Temperature ($^{\circ}\text{C}$)

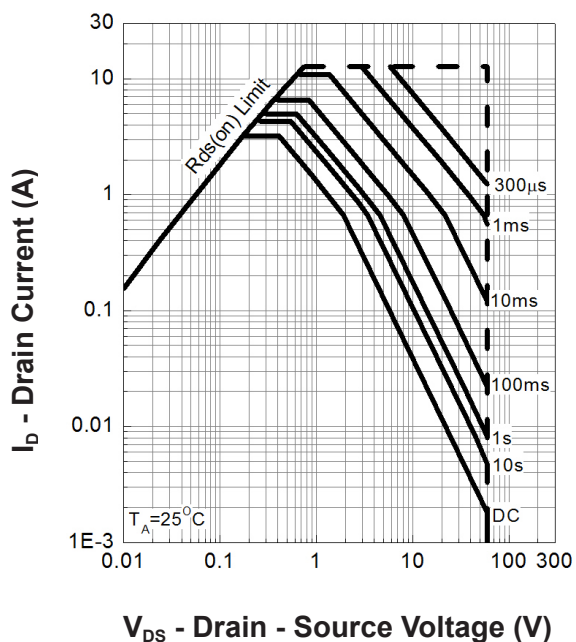
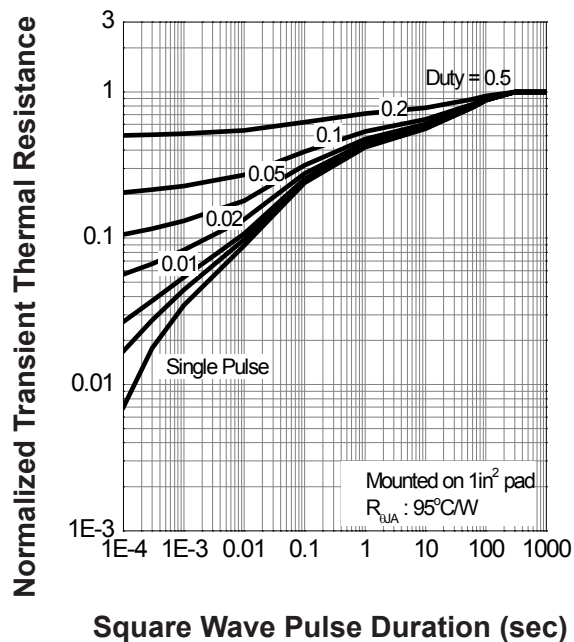
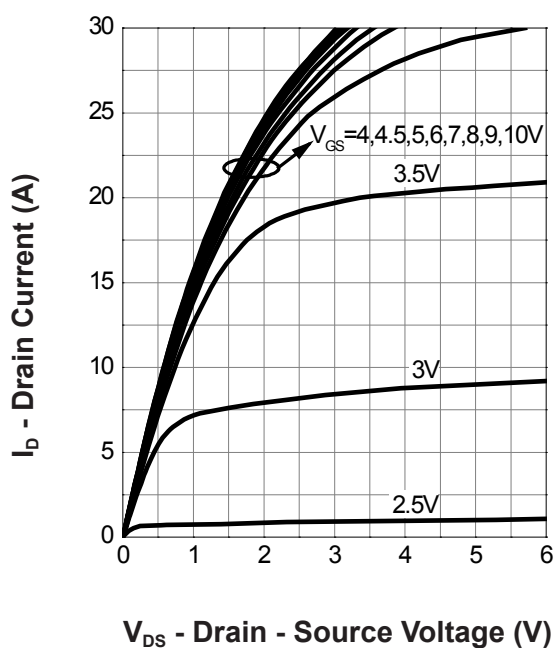
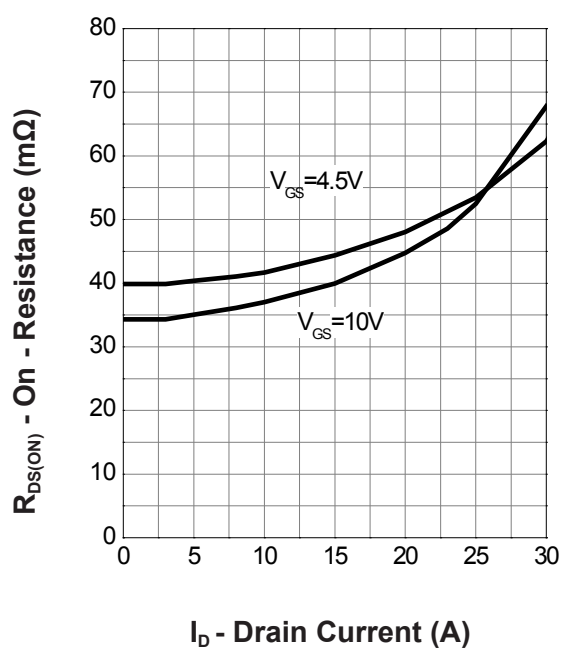
Drain Current

 T_c - Case Temperature ($^{\circ}\text{C}$)

Safe Operation Area

 V_{DS} - Drain - Source Voltage (V)

Thermal Transient Impedance


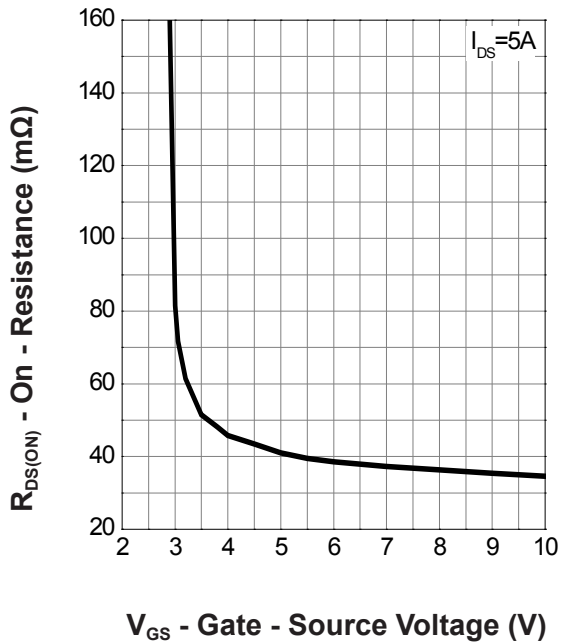
Square Wave Pulse Duration (sec)

N-Channel Typical Characteristics (Cont.)

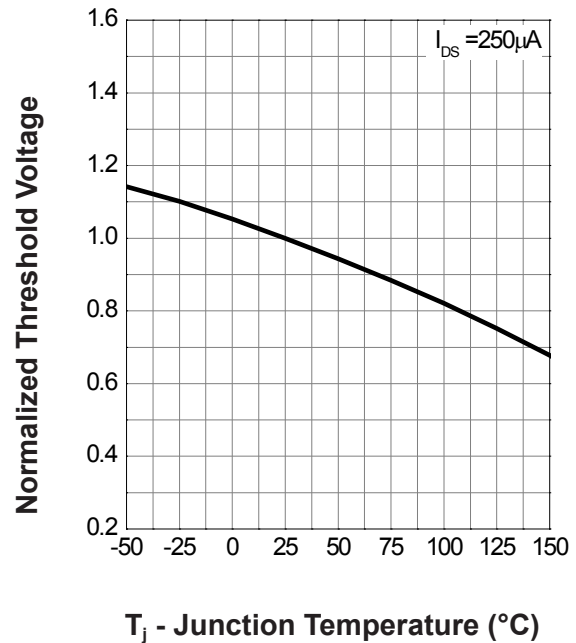
Safe Operation Area

Thermal Transient Impedance

Output Characteristics

Drain-Source On Resistance


N-Channel Typical Characteristics (Cont.)

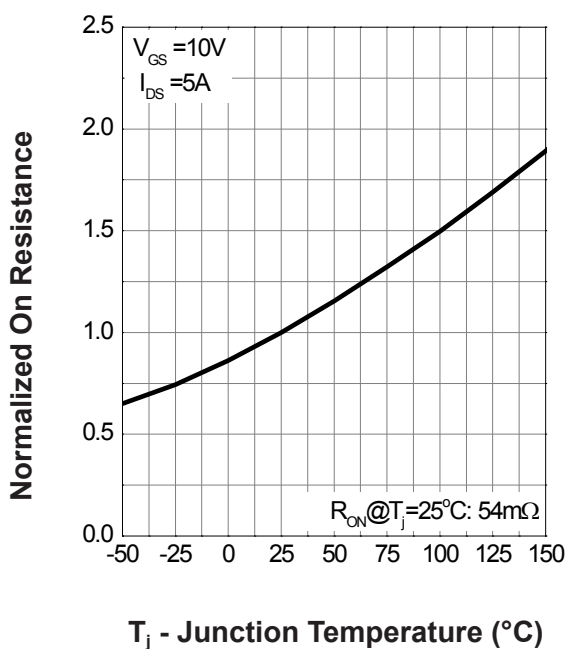
Gate-Source On Resistance



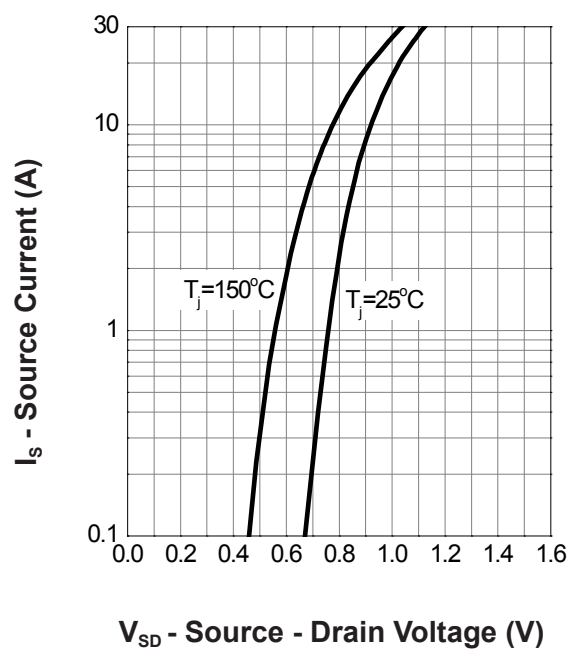
Gate Threshold Voltage



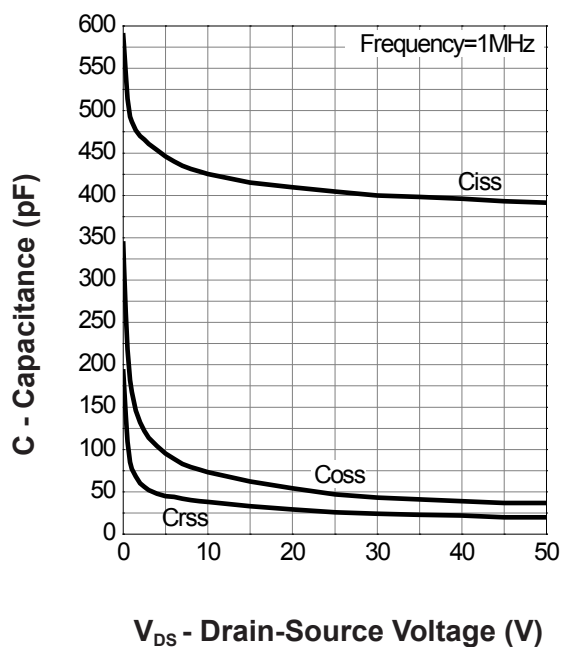
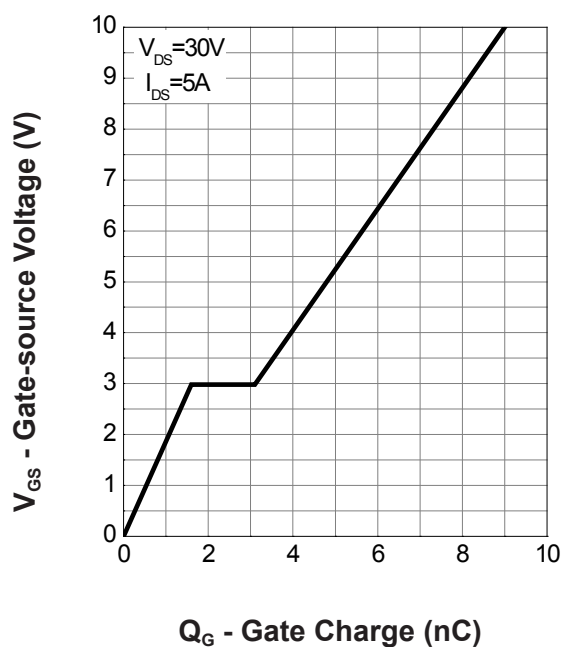
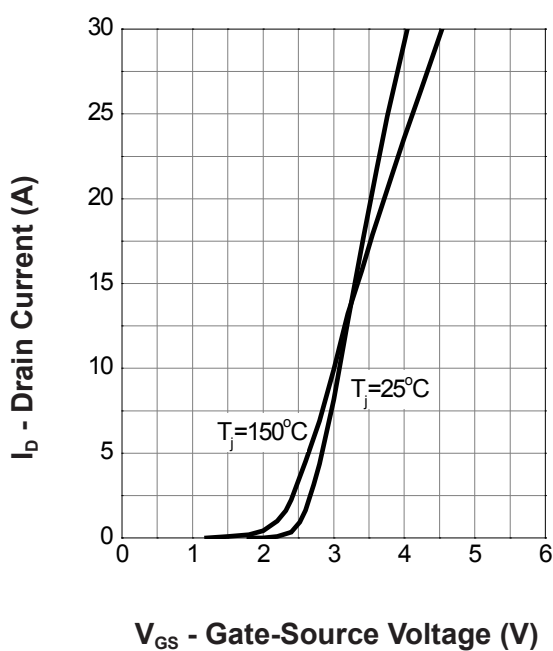
Drain-Source On Resistance



Source-Drain Diode Forward

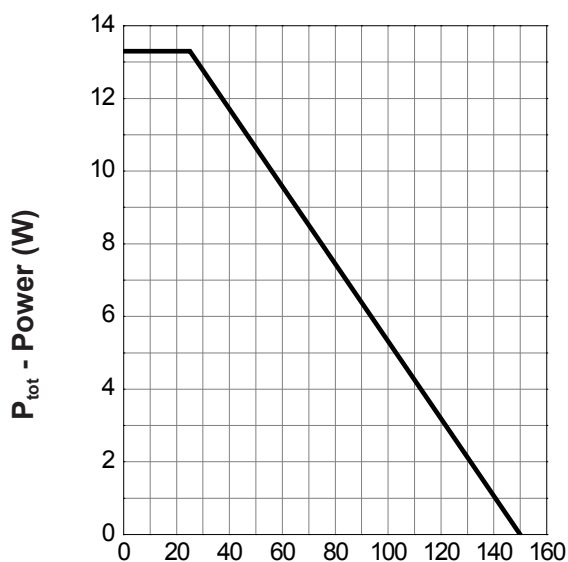


N-Channel Typical Characteristics (Cont.)

Capacitance

Gate Charge

Transfer Characteristics


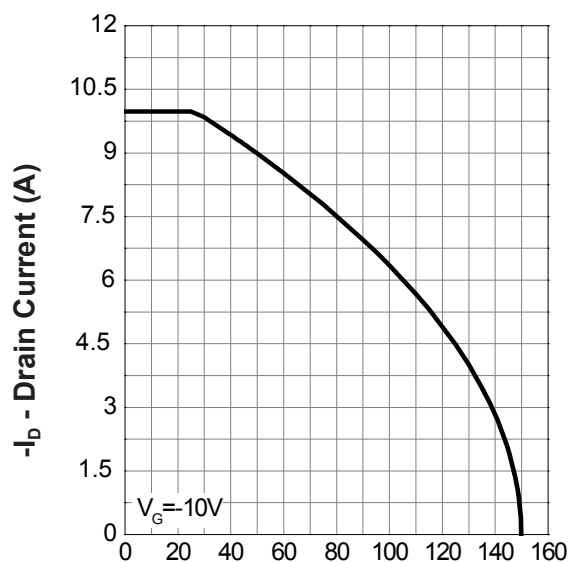
P-Channel Typical Characteristics

Power Dissipation



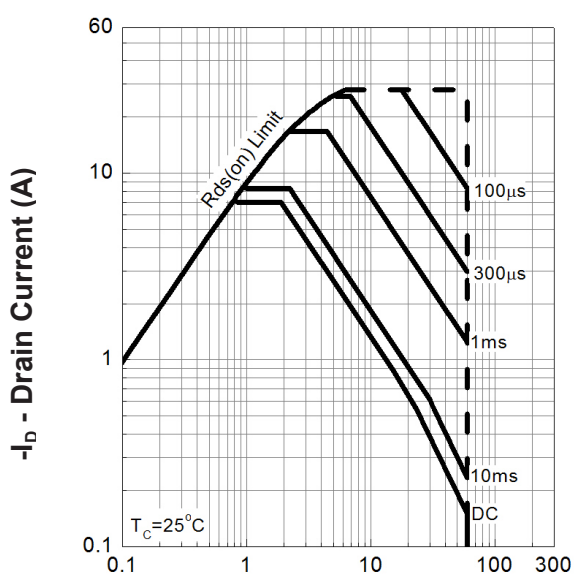
T_c - Case Temperature (°C)

Drain Current



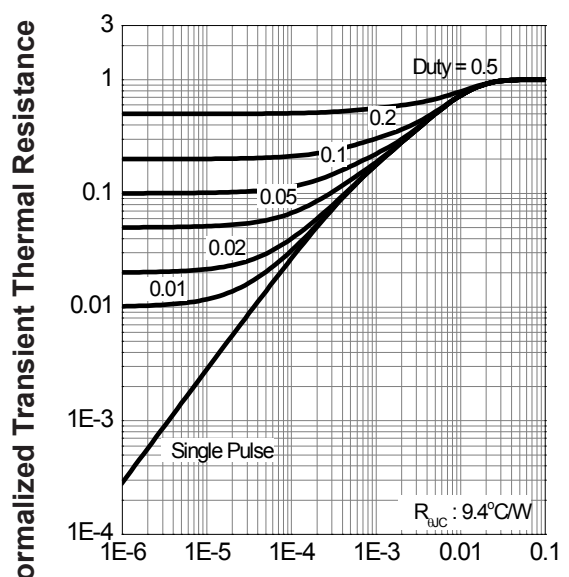
T_c - Case Temperature (°C)

Safe Operation Area



$-V_{DS}$ - Drain - Source Voltage (V)

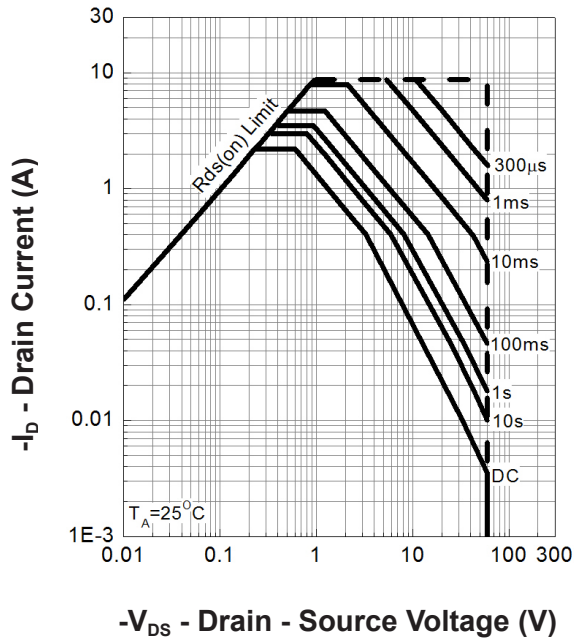
Thermal Transient Impedance



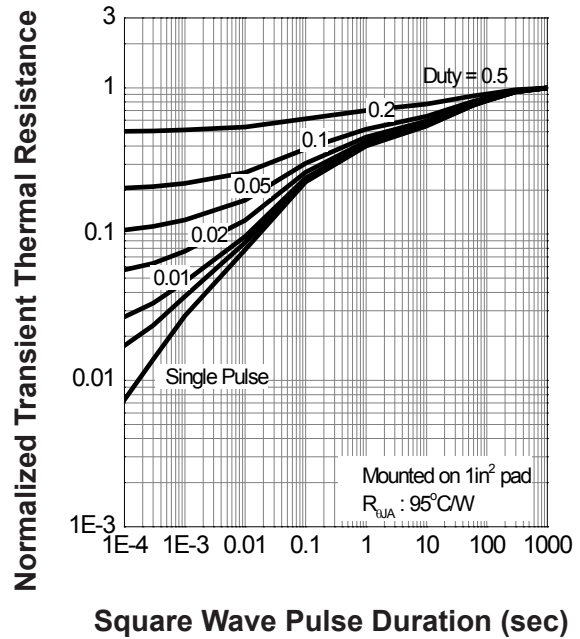
Square Wave Pulse Duration (sec)

P-Channel Typical Characteristics (Cont.)

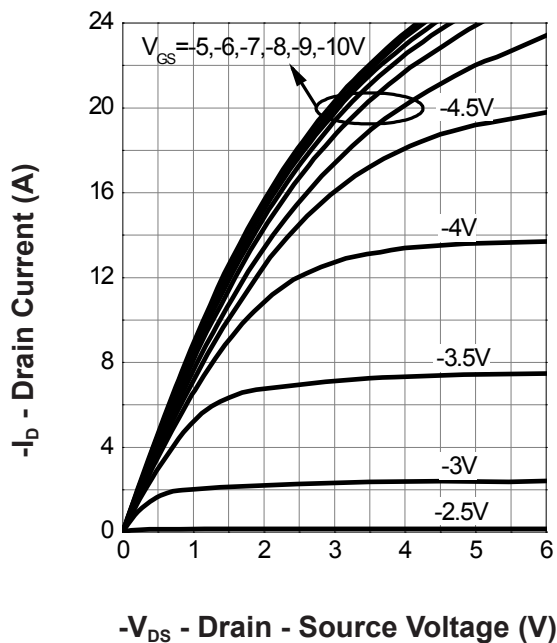
Safe Operation Area



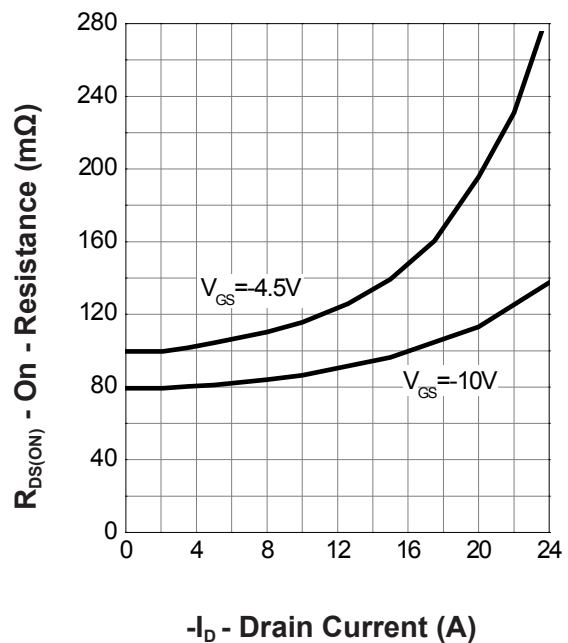
Thermal Transient Impedance

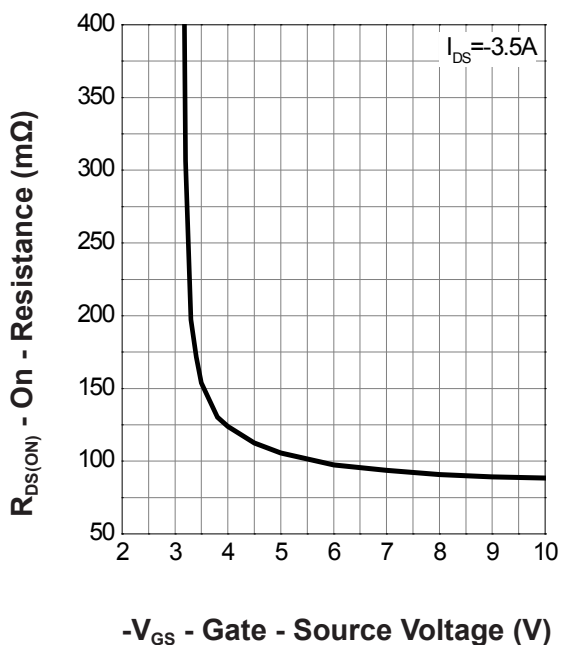
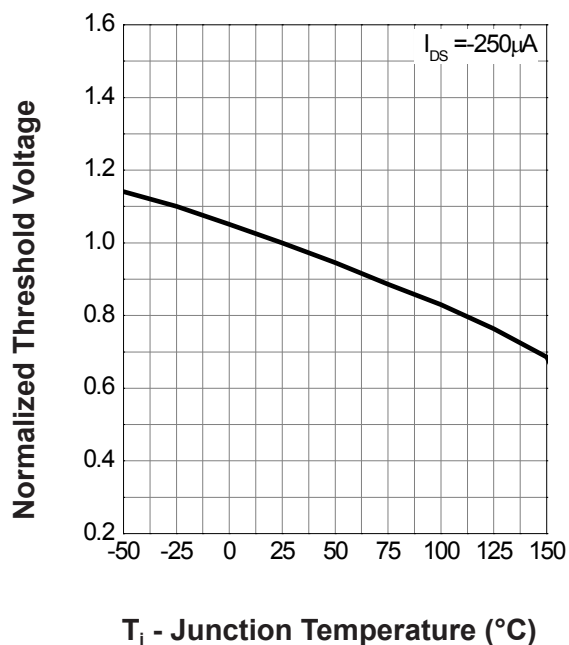
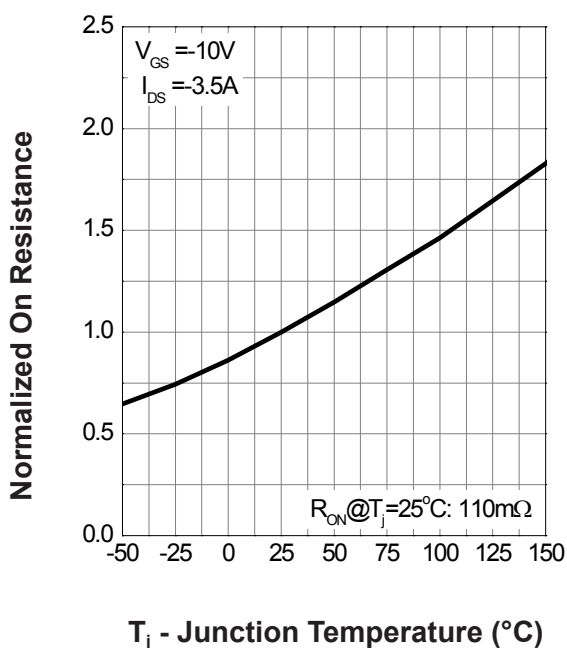
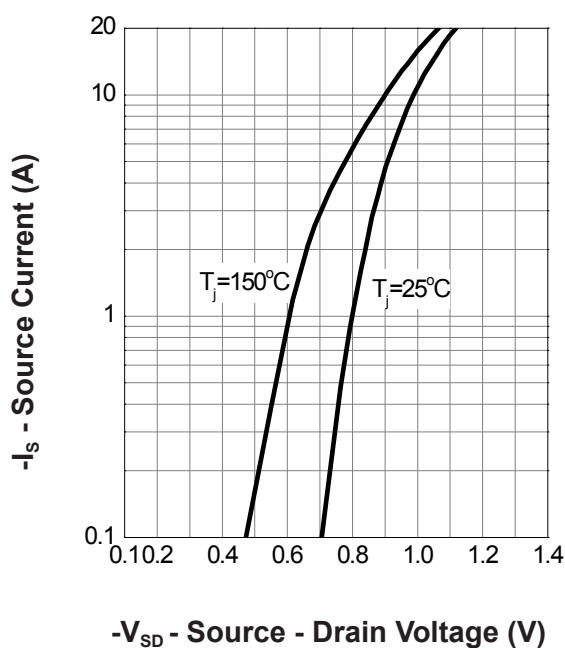


Output Characteristics



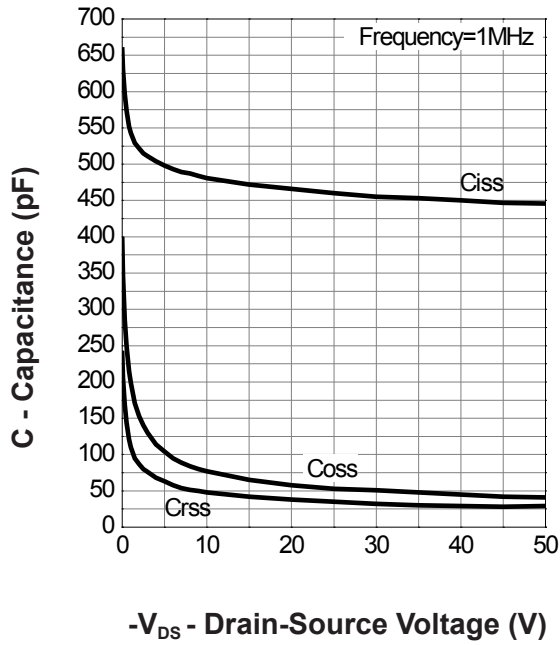
Drain-Source On Resistance



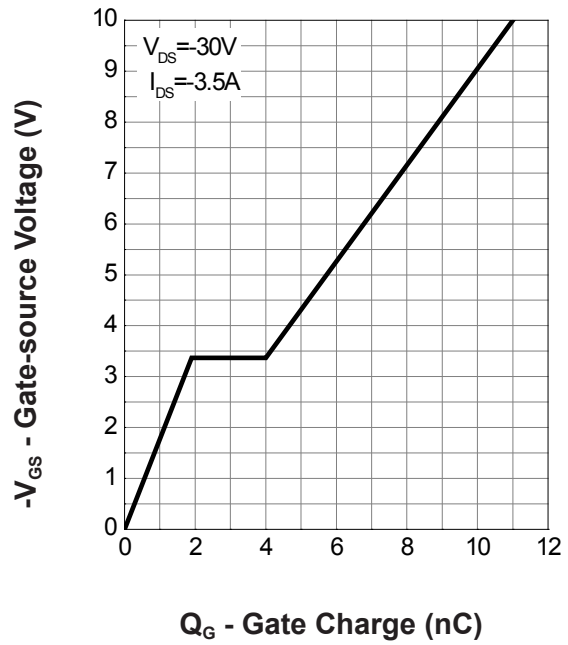
P-Channel Typical Characteristics (Cont.)
Gate-Source On Resistance

Gate Threshold Voltage

Drain-Source On Resistance

Source-Drain Diode Forward


P-Channel Typical Characteristics (Cont.)

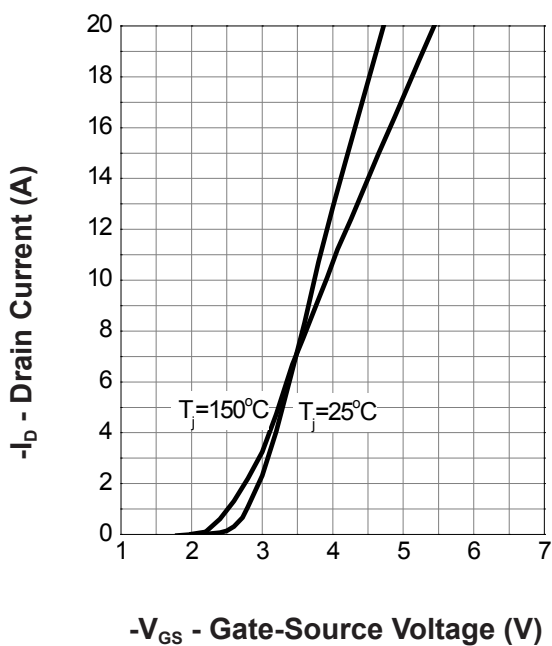
Capacitance



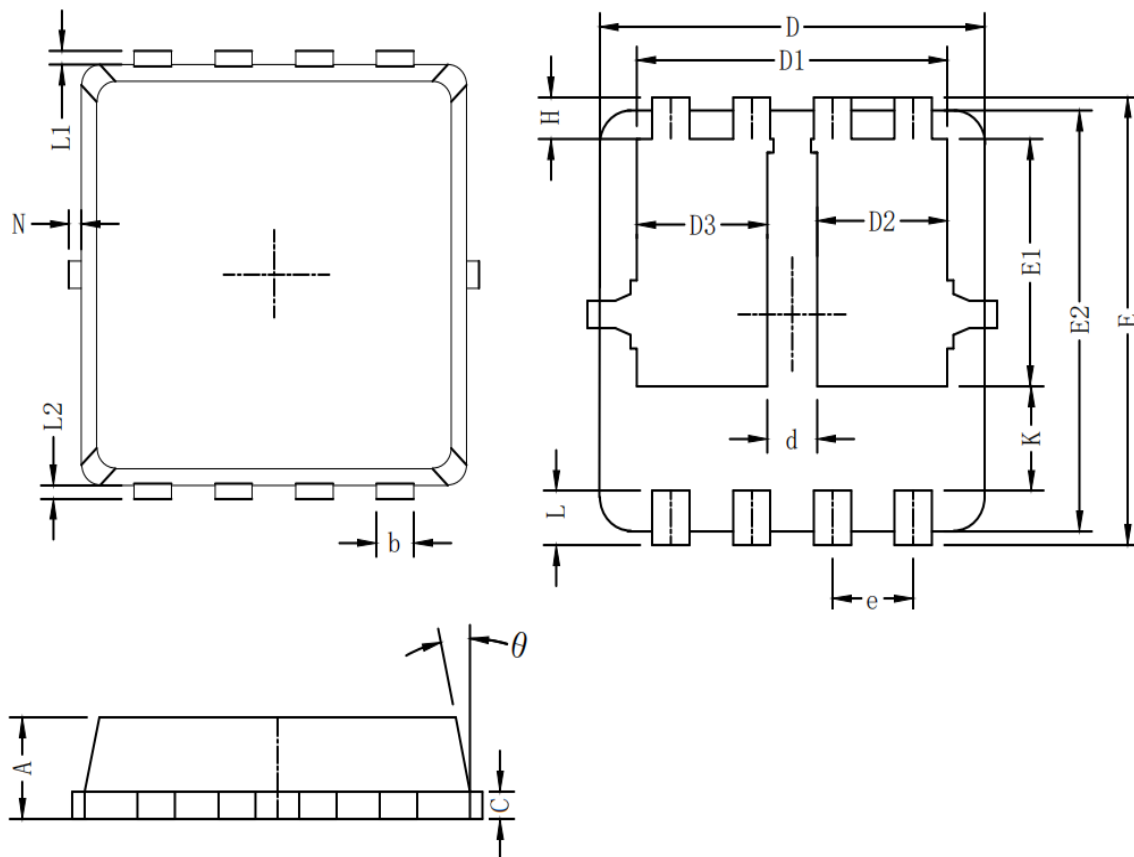
Gate Charge



Transfer Characteristics



Packaging information



Symbol	Dim in mm		
	min	typ	max
A	0.6	0.75	0.9
b	0.2	0.3	0.4
C	0.15	0.2	0.25
D	3	3.1	3.2
D1	2.3	2.45	2.6
D2/D3	0.8	1	1.2
E	3.15	3.3	3.45
E1	1.43	1.73	1.93
E2	2.9	3.05	3.2
e	0.65BSC		
H	0.2	0.35	0.5
K	0.57	0.77	0.87
L	0.3	0.4	0.5
L1/L2	0.1REF		
θ	8°	10°	13°
N	0		0.15
d	0.3	0.4	0.5



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