

General Description

The WSG02N20 is the highest performance trench N-Ch MOSFET with extreme high cell density, which provide excellent $R_{DS(on)}$ and gate charge for most of the small power switching and load switch applications.

The WSG02N20 meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent C_{dv}/dt effect decline
- Green Device Available

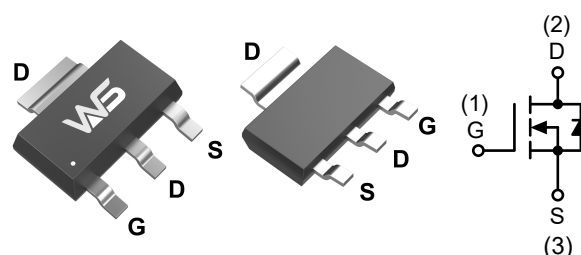
Product Summary

BV_{DSS}	$R_{DS(on)}$	I_D
200V	410m Ω	2A

Applications

- Power Management in TV Inverter.

SOT-223-3L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	200	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_c=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	2.0	A
$I_D@T_c=70^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	1.5	A
I_{DM}	Pulsed Drain Current ²	10	A
$P_D@T_A=25^{\circ}C$	Total Power Dissipation ³	18	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	---	70	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	30	$^{\circ}C/W$

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	200	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	0.098	---	V/ $^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=2A$	---	410	610	$m\Omega$
		$V_{GS}=6V, I_D=1A$	---	614	920	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	2.8	4.0	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.57	---	mV/ $^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=80V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=2A$	---	15	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	2.5	---	Ω
Q_g	Total Gate Charge (10V)	$V_{DS}=30V, V_{GS}=10V, I_D=2A$	---	51.7	---	nC
Q_{gs}	Gate-Source Charge		---	12.7	---	
Q_{gd}	Gate-Drain Charge		---	16.3	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V, V_{GEN}=10V, R_G=4.7\Omega, I_D=1A, R_L=17.7\Omega$	---	32	50	ns
T_r	Rise Time		---	32.1	51	
$T_{d(off)}$	Turn-Off Delay Time		---	5.2	10	
T_f	Fall Time		---	60.9	79	
C_{iss}	Input Capacitance	$V_{DS}=30V, V_{GS}=0V, f=1MHz$	---	645	---	pF
C_{oss}	Output Capacitance		---	68	---	
C_{rss}	Reverse Transfer Capacitance		---	21	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	2	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	10	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.15	V
t_{rr}	Reverse Recovery Time	$I_F=2A, di/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	38	---	nS
Q_{rr}	Reverse Recovery Charge		---	56	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, $t \leq 10\text{sec}$.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

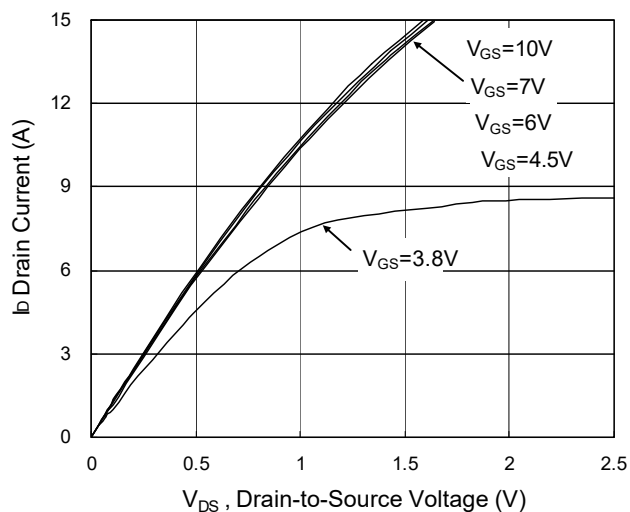


Fig.1 Typical Output Characteristics

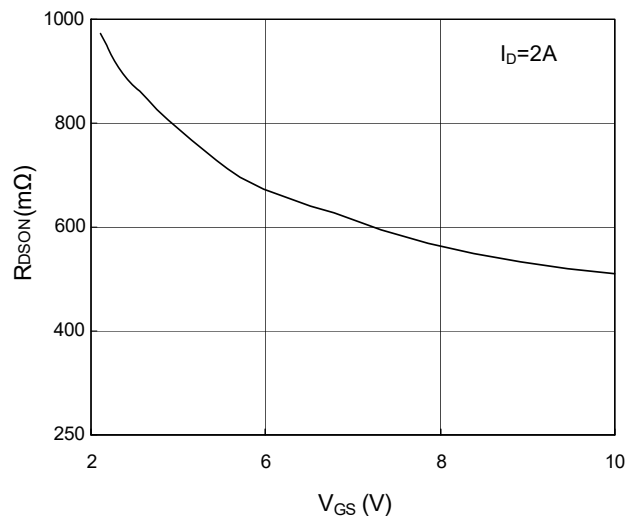


Fig.2 On-Resistance vs. Gate-Source

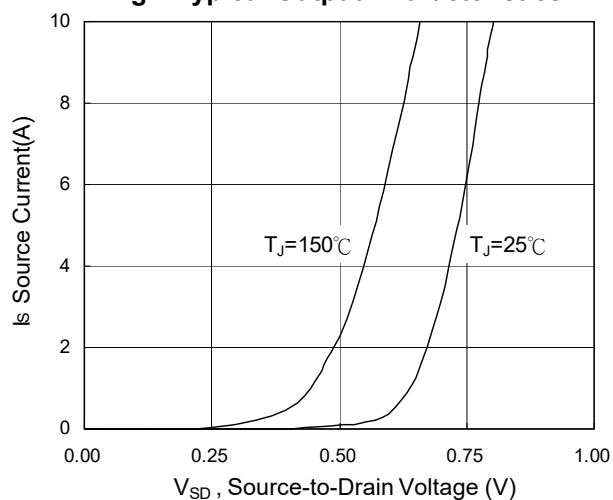


Fig.3 Forward Characteristics Of Reverse

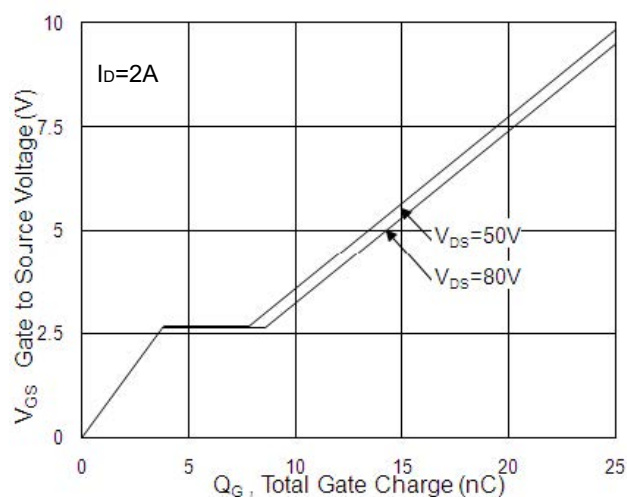


Fig.4 Gate-Charge Characteristics

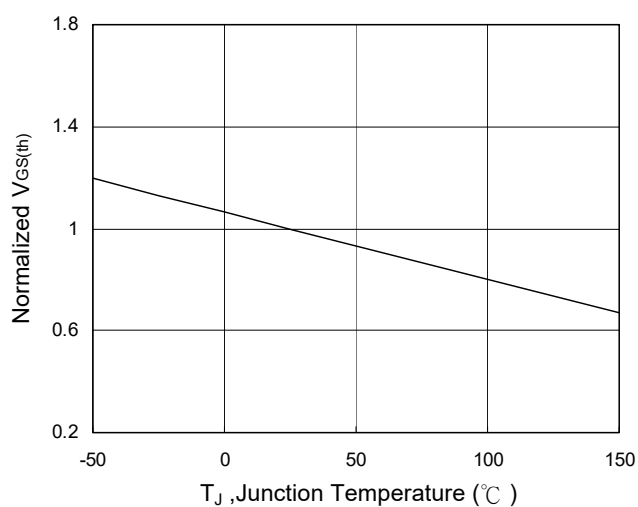


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

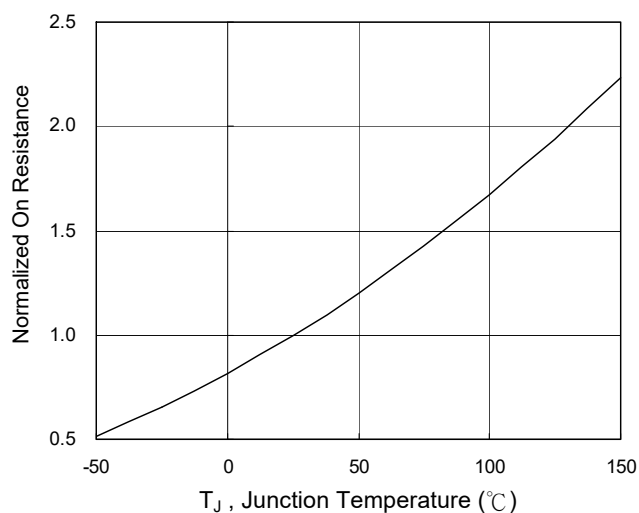


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

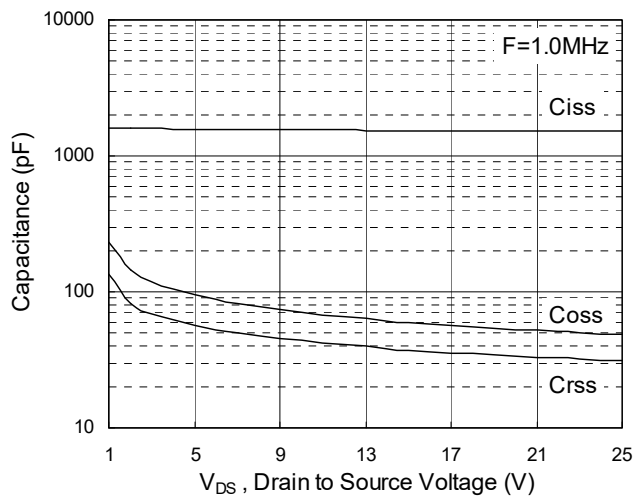


Fig.7 Capacitance

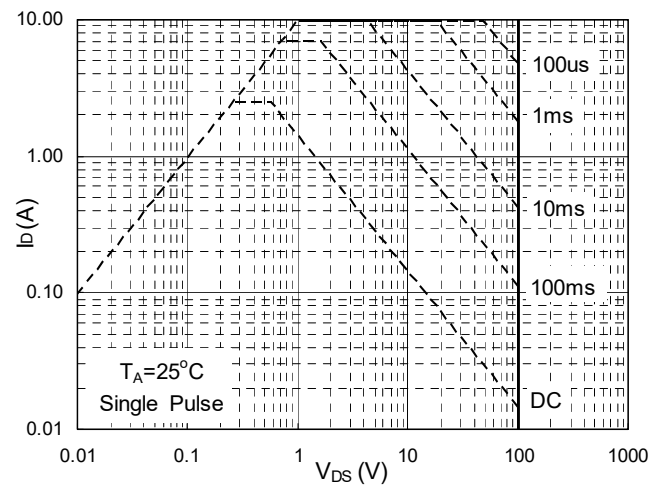


Fig.8 Safe Operating Area

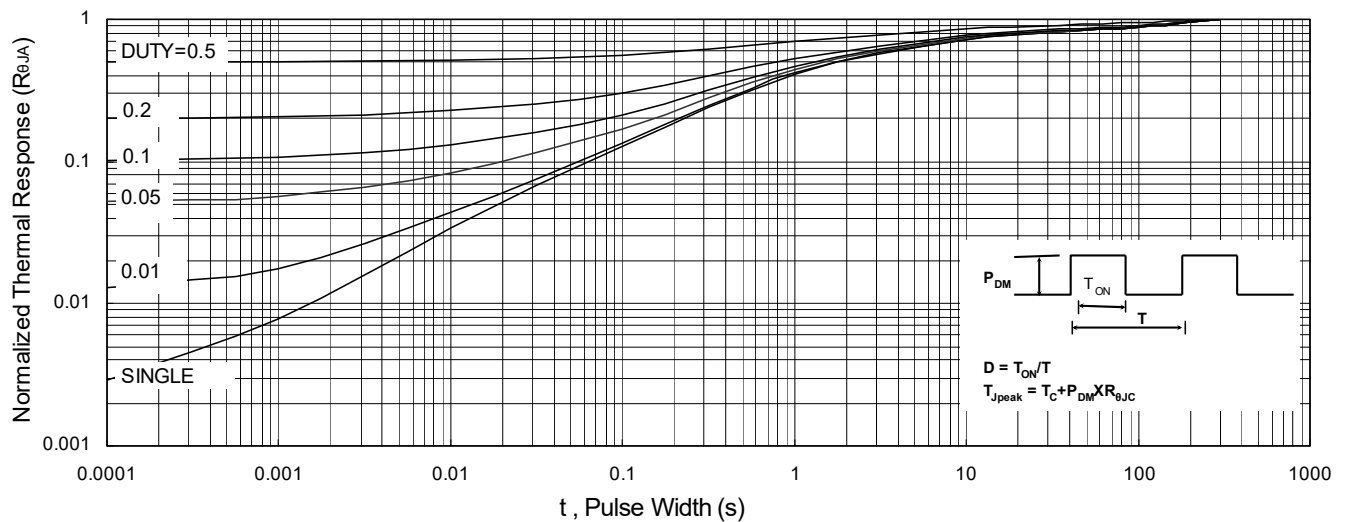


Fig.9 Normalized Maximum Transient Thermal Impedance

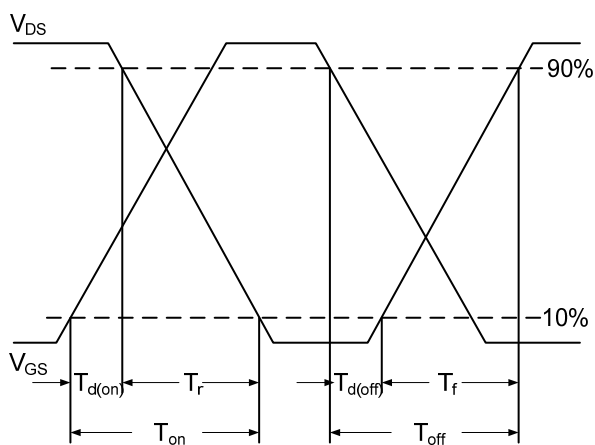


Fig.10 Switching Time Waveform

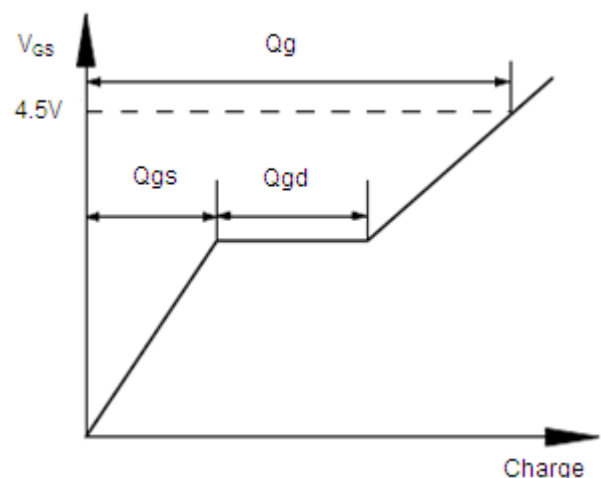
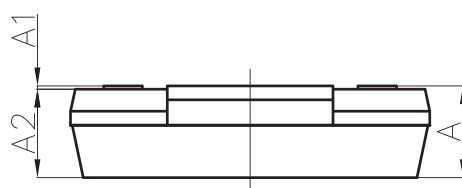
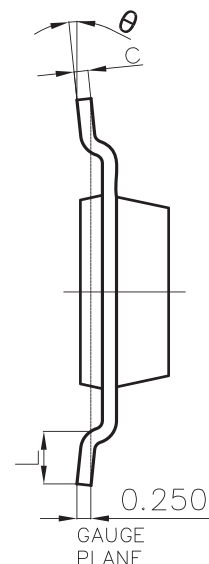
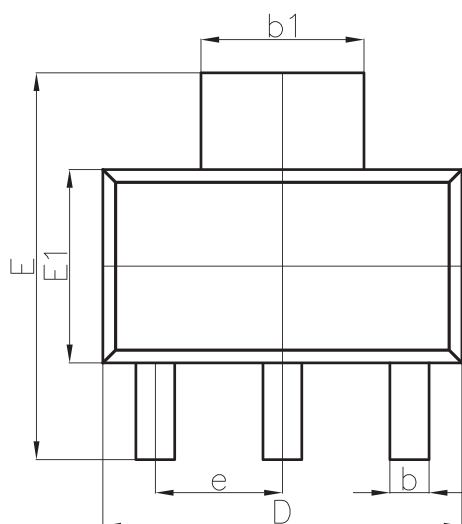


Fig.11 Gate Charge Waveform

Packaging information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	—	1.800	—	0.071
A1	0.020	0.100	0.001	0.004
A2	1.500	1.700	0.059	0.067
b	0.660	0.840	0.026	0.033
b1	2.900	3.100	0.114	0.122
c	0.230	0.350	0.009	0.014
D	6.300	6.700	0.248	0.264
E	6.700	7.300	0.264	0.287
E1	3.300	3.700	0.130	0.146
e	2.300 (BSC)		0.091 (BSC)	
L	0.750	—	0.030	—
θ	0°	10°	0°	10°

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