

### General Description

The WST02P06 is the highest performance trench P-ch MOSFET with extreme high cell density, which provide excellent  $R_{DS(ON)}$  and gate charge for most of the small power switching and load switch applications.

The WST02P06 meet the RoHS and Green Product requirement with full function reliability approved.

### Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent  $CdV/dt$  effect decline
- 100% EAS Guaranteed
- Green Device Available

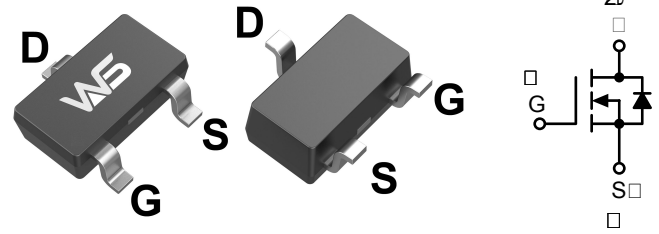
### Product Summary

$BV_{DSS}$	$R_{DS(ON)}$	$I_D$
-60V	165m $\Omega$	-2.8A

### Applications

- High Frequency Point-of-Load Synchronous Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

### SOT23/ Pin Configuration



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-60	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $-V_{GS} @ -10V^1$	-2.8	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $-V_{GS} @ -10V^1$	-1.8	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-8.4	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>3</sup>	1.5	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	125	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	80	$^\circ C/W$

**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-60	---	---	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =-1mA	---	-0.021	---	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-1.5A	---	165	200	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-1A	---	200	260	
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.1	-1.7	-2.5	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient		---	4.08	---	mV/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-48V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =-48V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =-10V, I <sub>D</sub> =-1.5A	---	5.5	---	S
Q <sub>g</sub>	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-20V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-1.5A	---	4.6	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	1.4	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	1.6	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =-15V, V <sub>GS</sub> =-10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-1A	---	17.4	---	ns
T <sub>r</sub>	Rise Time		---	5.4	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	37.2	---	
T <sub>f</sub>	Fall Time		---	2.4	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz	---	456	---	pF
C <sub>oss</sub>	Output Capacitance		---	59	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	38	---	

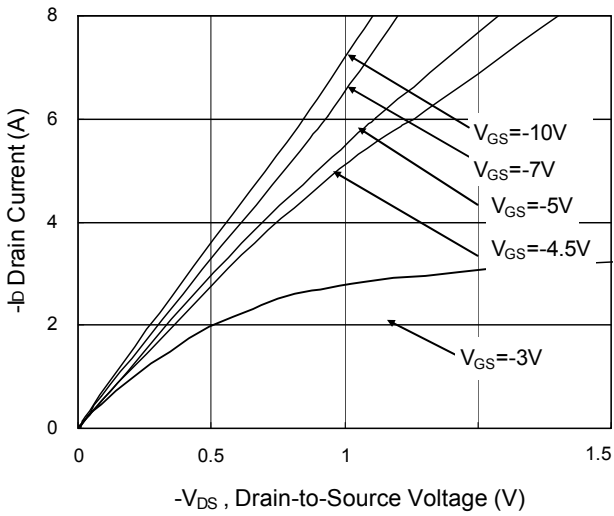
**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1,4</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	-2.8	A
I <sub>SM</sub>	Pulsed Source Current <sup>2,4</sup>		---	---	-7.1	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A, T <sub>J</sub> =25°C	---	---	-1.2	V

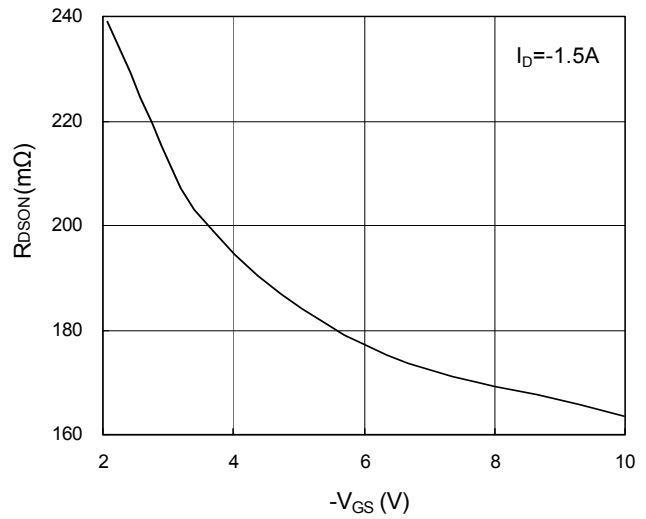
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper,t<10sec.
- 2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications , should be limited by total power dissipation.

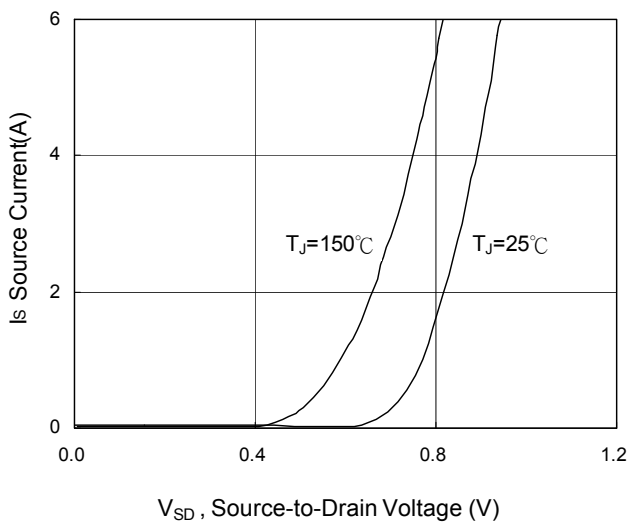
**Typical Characteristics**



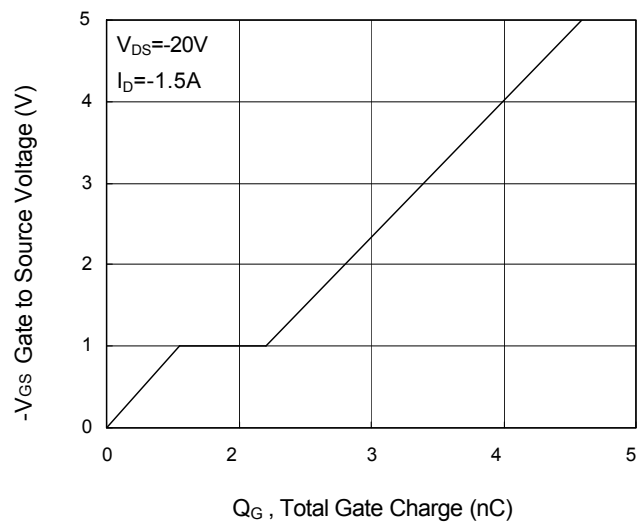
**Fig.1 Typical Output Characteristics**



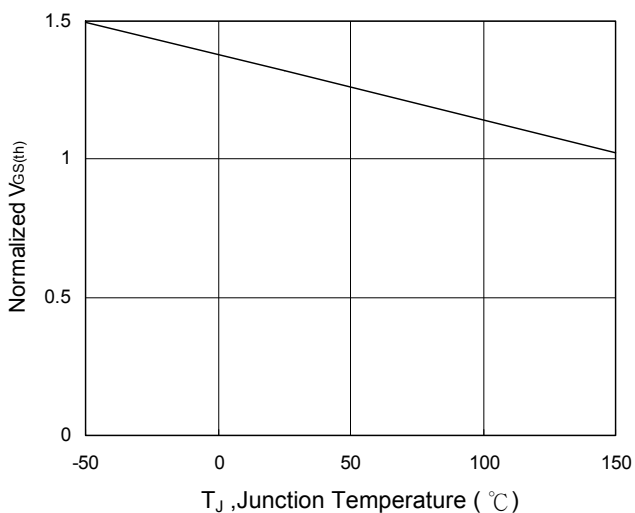
**Fig.2 On-Resistance v.s Gate-Source**



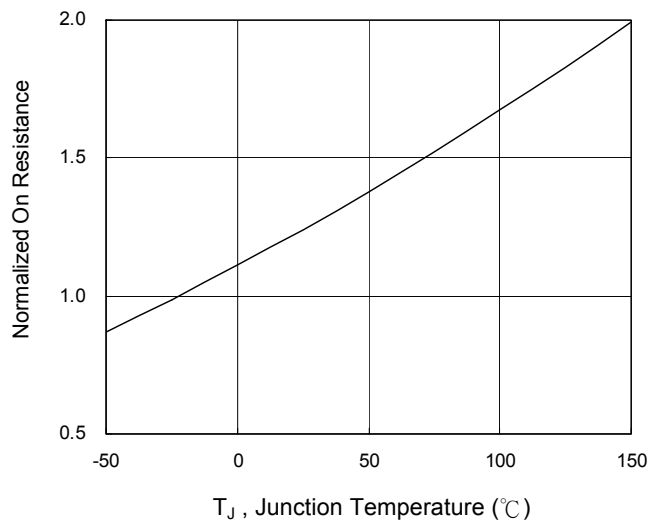
**Fig.3 Forward Characteristics Of Reverse**



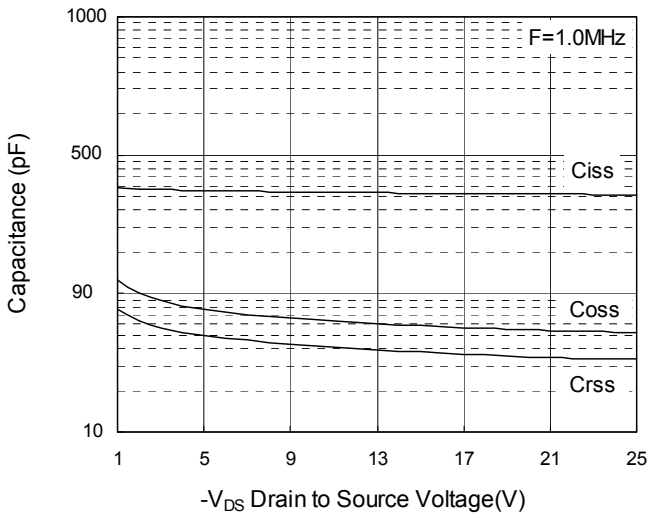
**Fig.4 Gate-Charge Characteristics**



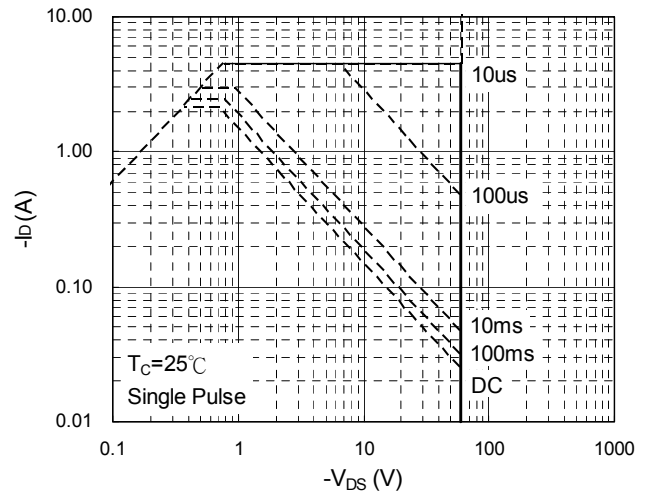
**Fig.5 Normalized V<sub>GS(th)</sub> v.s T<sub>J</sub>**



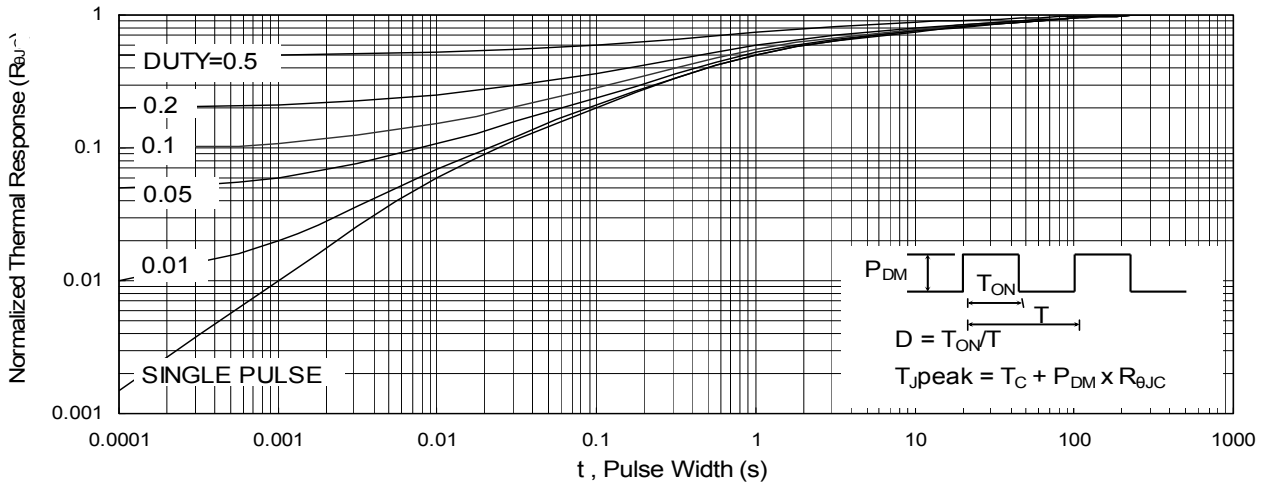
**Fig.6 Normalized R<sub>DS(on)</sub> v.s T<sub>J</sub>**



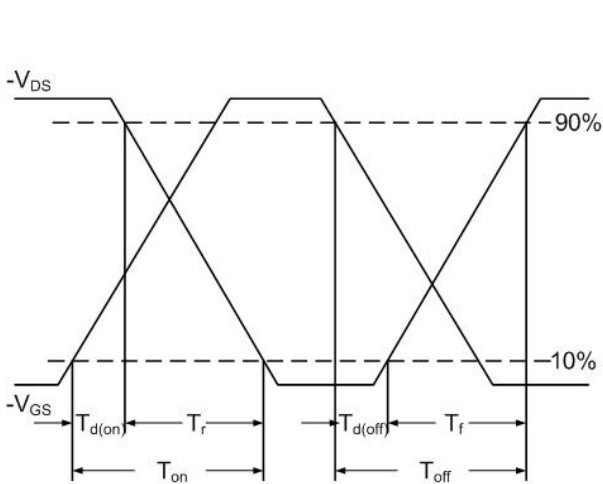
**Fig.7 Capacitance**



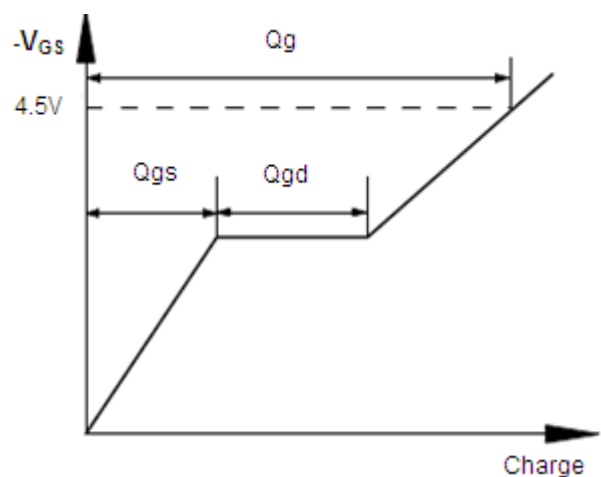
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching time waveform**



**Fig.11 Gate Charge waveform**



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