

## General Description

The WST2007 is the highest performance trench P-ch MOSFET with extreme high cell density , which provide excellent  $R_{DS(on)}$  and gate charge for most of the small power switching and load switch applications.

The WST2007 meet the RoHS and Green Product requirement with full function reliability approved.

## Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent  $C_{dv}/dt$  effect decline
- Green Device Available

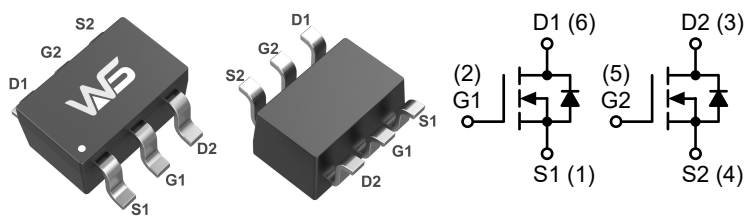
## Product Summary

$BV_{DSS}$	$R_{DS(on)}$	$I_D$
20V	140m $\Omega$	1.4 A

## Applications

- High Frequency Point-of-Load Synchronous  
Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

## SOT-363-6L Pin Configuration



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	20	V
$V_{GS}$	Gate-Source Voltage	$\pm 8$	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	1.4	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	1.1	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	7.2	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation <sup>3</sup>	0.33	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup>	---	375	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	240	$^\circ\text{C}/\text{W}$

**Electrical Characteristics ( $T_J=25^{\circ}\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V$ , $I_D=250\mu A$	20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to $25^{\circ}\text{C}$ , $I_D=1mA$	---	0.02	---	V/ $^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=4.5V$ , $I_D=1.5A$	---	140	450	m $\Omega$
		$V_{GS}=2.5V$ , $I_D=1A$	---	180	765	
		$V_{GS}=1.8V$ , $I_D=0.8A$	---	270	850	m $\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$ , $I_D=250\mu A$	0.3	0.6	1	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-2.5	---	mV/ $^{\circ}\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=16V$ , $V_{GS}=0V$ , $T_J=25^{\circ}\text{C}$	---	---	1	$\mu A$
		$V_{DS}=16V$ , $V_{GS}=0V$ , $T_J=55^{\circ}\text{C}$	---	---	5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 8V$ , $V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=5V$ , $I_D=1A$	---	6	---	S
$R_g$	Gate Resistance	$V_{DS}=0V$ , $V_{GS}=0V$ , $f=1MHz$	---	2	4	$\Omega$
$Q_g$	Total Gate Charge (4.5V)	$V_{DS}=15V$ , $V_{GS}=4.5V$ , $I_D=1A$	---	3.3	4.6	nC
$Q_{gs}$	Gate-Source Charge		---	0.51	0.7	
$Q_{gd}$	Gate-Drain Charge		---	0.88	1.2	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=10V$ , $V_{GS}=4.5V$ , $R_G=3.3\Omega$ , $I_D=1A$	---	2	4.0	ns
$T_r$	Rise Time		---	29.2	53	
$T_{d(off)}$	Turn-Off Delay Time		---	6.8	13.6	
$T_f$	Fall Time		---	10	20	
$C_{iss}$	Input Capacitance	$V_{DS}=15V$ , $V_{GS}=0V$ , $f=1MHz$	---	204	286	pF
$C_{oss}$	Output Capacitance		---	43.6	61	
$C_{rss}$	Reverse Transfer Capacitance		---	30	42	

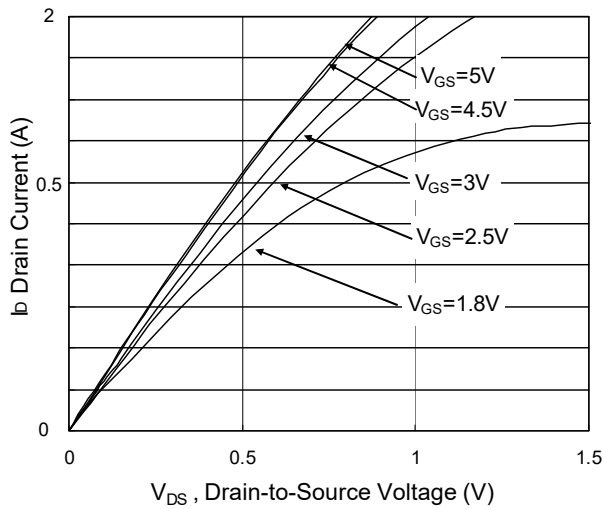
**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V$ , Force Current	---	---	1.4	A
$I_{SM}$	Pulsed Source Current <sup>2,4</sup>		---	---	7.2	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V$ , $I_S=1A$ , $T_J=25^{\circ}\text{C}$	---	---	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F=2A$ , $di/dt=100A/\mu s$ , $T_J=25^{\circ}\text{C}$	---	3.9	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	1.04	---	nC

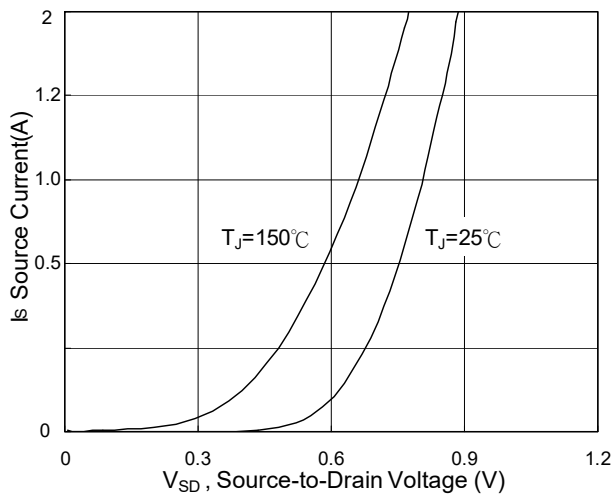
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
- 3.The power dissipation is limited by  $150^{\circ}\text{C}$  junction temperature
- 4.The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications , should be limited by total power dissipation.

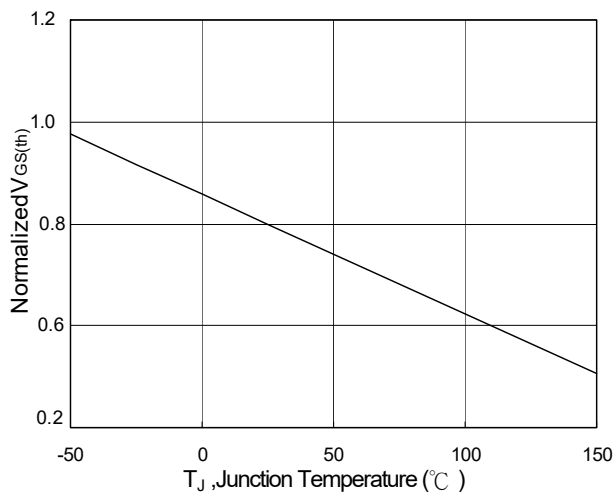
## Typical Characteristics



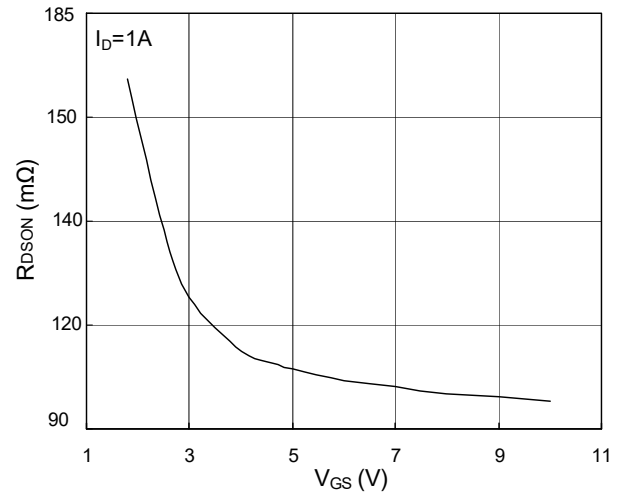
**Fig.1 Typical Output Characteristics**



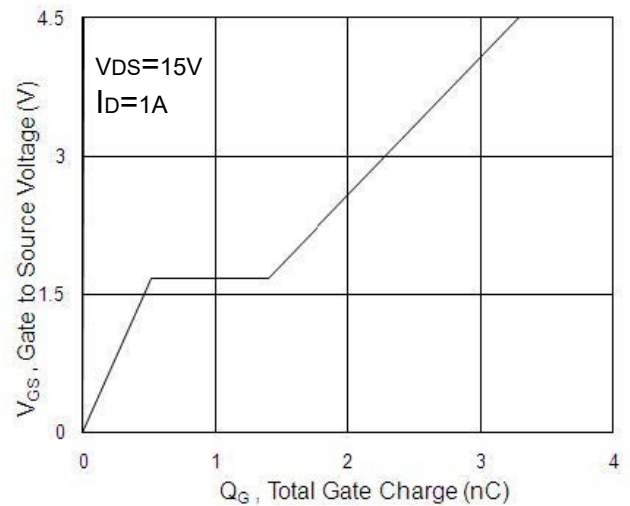
**Fig.3 Forward Characteristics Of Reverse**



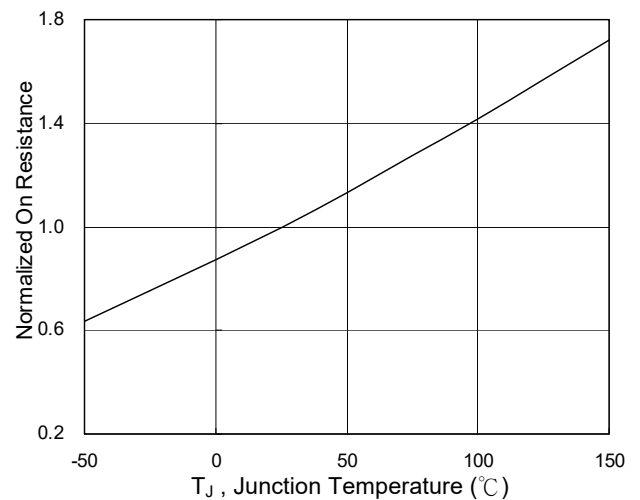
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



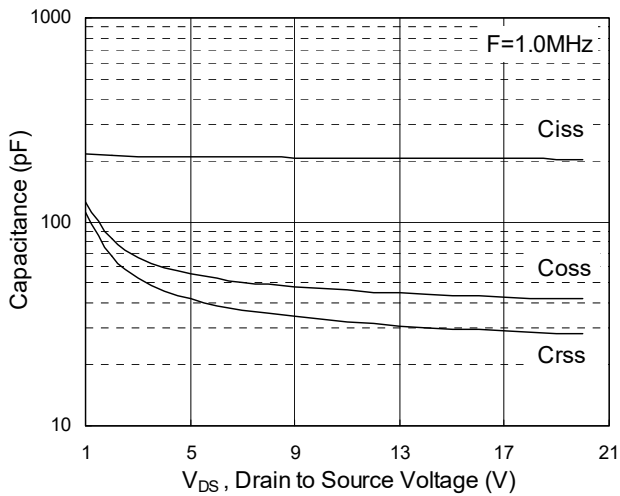
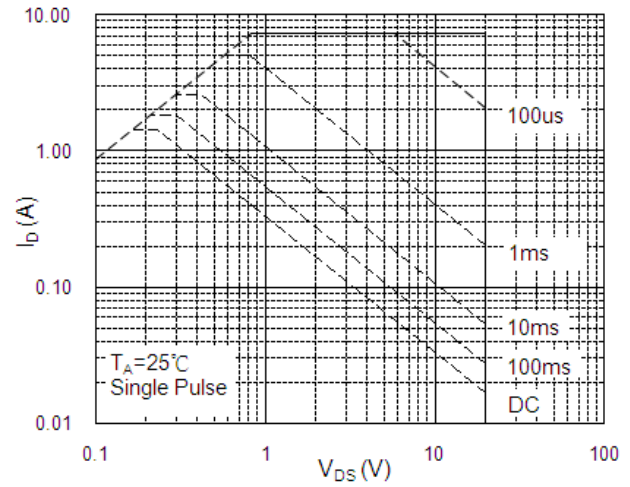
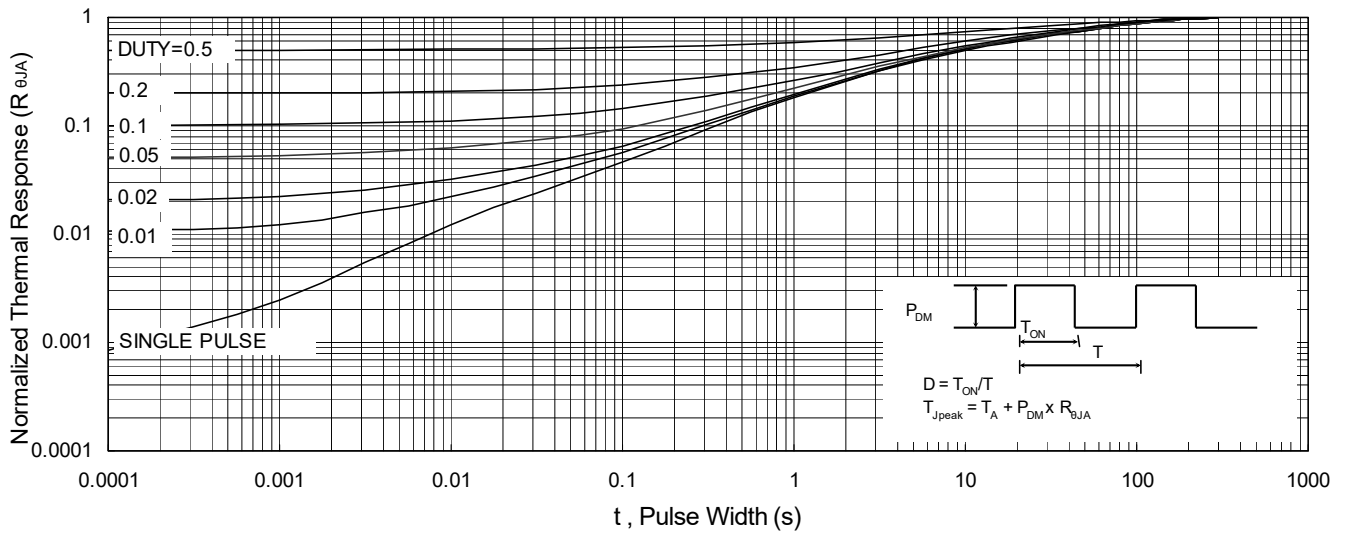
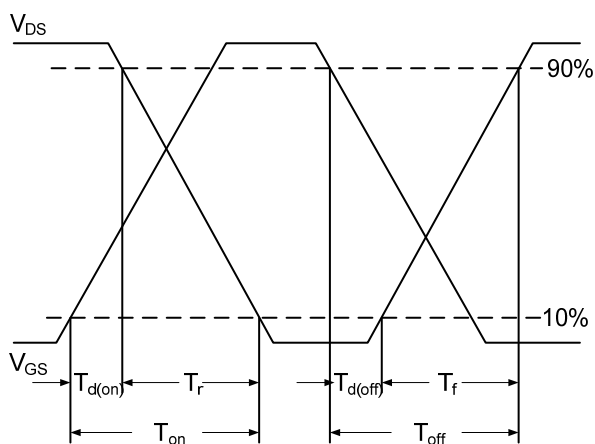
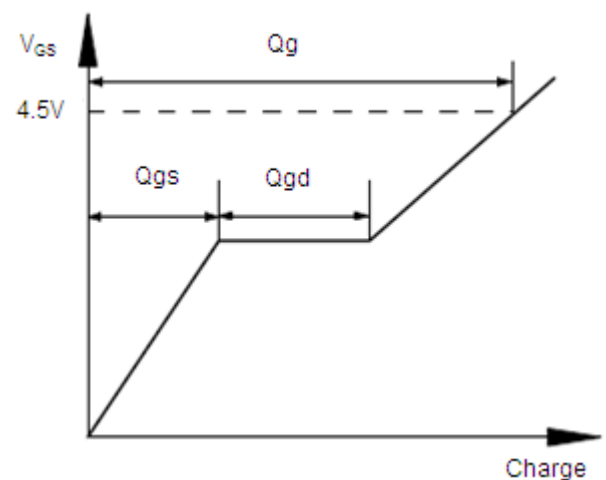
**Fig.2 On-Resistance vs. Gate-Source**



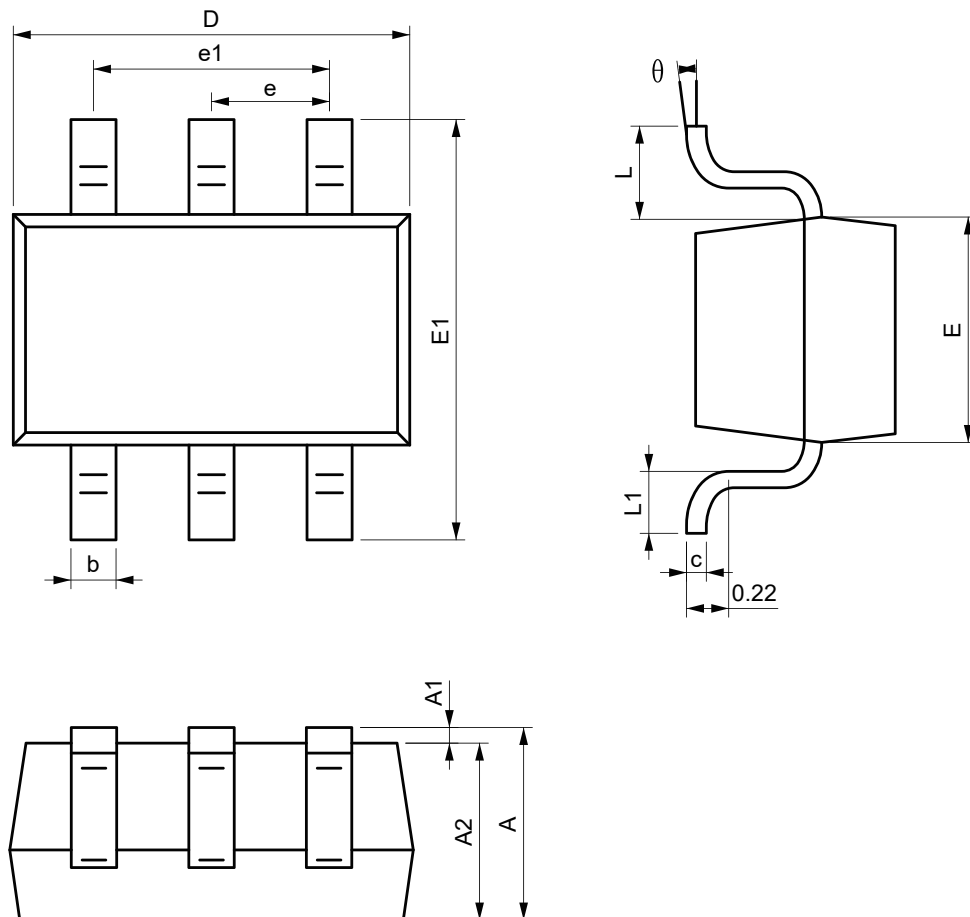
**Fig.4 Gate-Charge Characteristics**



**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**


**Fig.7 Capacitance**

**Fig.8 Safe Operating Area**

**Fig.9 Normalized Maximum Transient Thermal Impedance**

**Fig.10 Switching Time Waveform**

**Fig.11 Gate Charge Waveform**

## Packaging information



Symbol	Dimension in Millimeters	
	Min	Max
A	0.900	1.100
A1	0.000	0.100
A2	0.600	1.000
b	0.150	0.350
c	0.080	0.150
D	2.000	2.200
E	1.150	1.350
E1	2.150	2.450
e	0.650TYP	
e1	1.200	1.400
L	0.525REF	
L1	0.260	0.460
$\theta$	0°	8°

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