

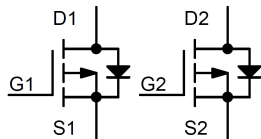
### General Description

The WST2011 is the highest performance trench P-ch MOSFETs with extreme high cell density , which provide excellent RDSON and gate charge for most of the small power switching and load switch applications.

The WST2011 meet the RoHS and Green Product requirement with full function reliability approved.

### Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Green Device Available



### Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		10s	Steady State	
$V_{DS}$	Drain-Source Voltage	-20		V
$V_{GS}$	Gate-Source Voltage	$\pm 12$		V
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-3.6	-3.2	A
$I_D@T_A=70^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V^1$	-2.6	-2.4	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-12		A
$P_D@T_A=25^\circ C$	Total Power Dissipation <sup>3</sup>	1.7	1.4	W
$P_D@T_A=70^\circ C$	Total Power Dissipation <sup>3</sup>	1.2	0.9	W
$T_{STG}$	Storage Temperature Range	-55 to 150		$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150		$^\circ C$

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	125	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup> ( $t \leq 10s$ )	---	95	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	80	$^\circ C/W$

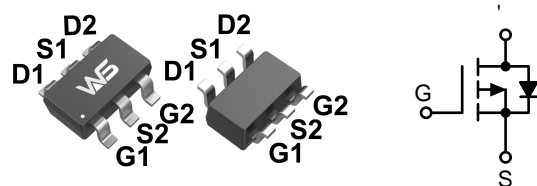
### Product Summary

BVDSS	RDSON	ID
-20V	80m $\Omega$	-3.2A

### Applications

- High Frequency Point-of-Load Synchronous Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

### SOT-23-6L Pin Configuration



**Electrical Characteristics ( $T_J=25^\circ\text{C}$ , unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-20	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	$BV_{DSS}$ Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$	---	-0.011	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-4.5V, I_D=-2A$	---	80	85	$\text{m}\Omega$
		$V_{GS}=-2.5V, I_D=-1A$	---	95	115	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-0.5	-1.0	-1.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	3.95	---	$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Drain-Source Leakage Current	$V_{DS}=-16V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	$\mu A$
		$V_{DS}=-16V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS}=\pm 12V, V_{DS}=0V$	---	---	$\pm 100$	nA
$g_{fs}$	Forward Transconductance	$V_{DS}=-5V, I_D=-2A$	---	8.5	---	S
$Q_g$	Total Gate Charge (-4.5V)	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-2A$	---	3.3	11.3	nC
$Q_{gs}$	Gate-Source Charge		---	1.1	1.7	
$Q_{gd}$	Gate-Drain Charge		---	1.1	2.9	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-4.5V,$ $R_G=3.3\Omega, I_D=-2A$	---	7.2	---	ns
$T_r$	Rise Time		---	9.3	---	
$T_{d(off)}$	Turn-Off Delay Time		---	15.4	---	
$T_f$	Fall Time		---	3.6	---	
$C_{iss}$	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	750	---	pF
$C_{oss}$	Output Capacitance		---	95	---	
$C_{rss}$	Reverse Transfer Capacitance		---	68	---	

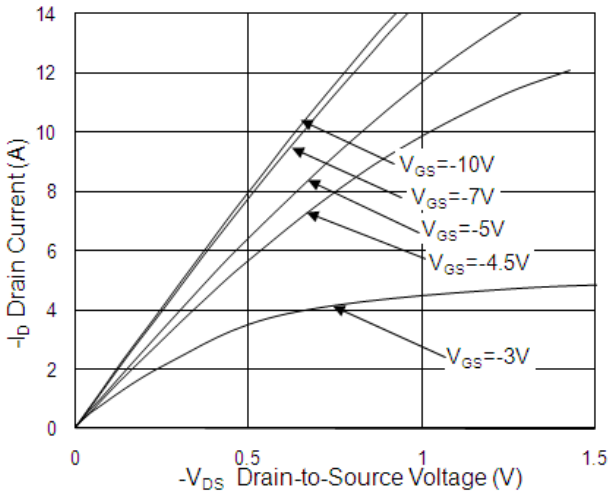
**Diode Characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous Source Current <sup>1,4</sup>	$V_G=V_D=0V$ , Force Current	---	---	-1.0	A
$I_{SM}$	Pulsed Source Current <sup>2,4</sup>		---	---	-12	A
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.1	V
$t_{rr}$	Reverse Recovery Time	$I_F=-2A, dI/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	19	---	nS
$Q_{rr}$	Reverse Recovery Charge		---	14	---	nC

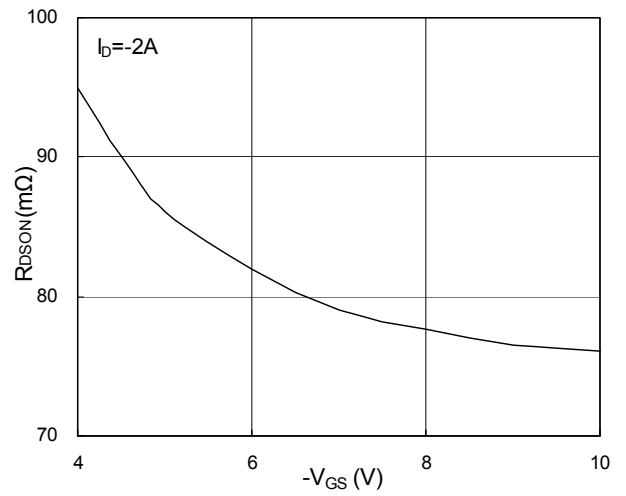
Note :

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
- 3.The power dissipation is limited by  $150^\circ\text{C}$  junction temperature
- 4.The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

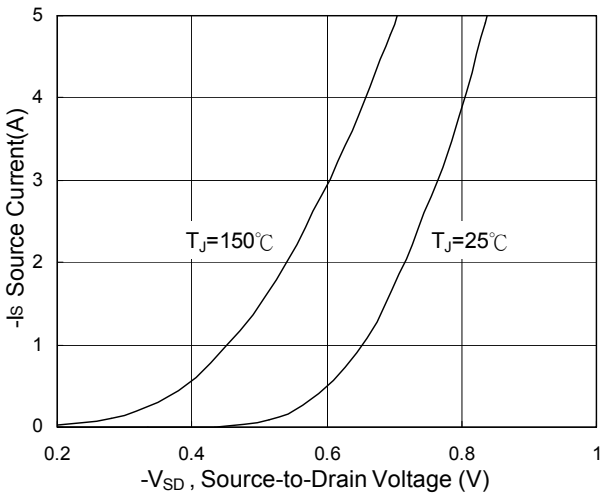
**Typical Characteristics**



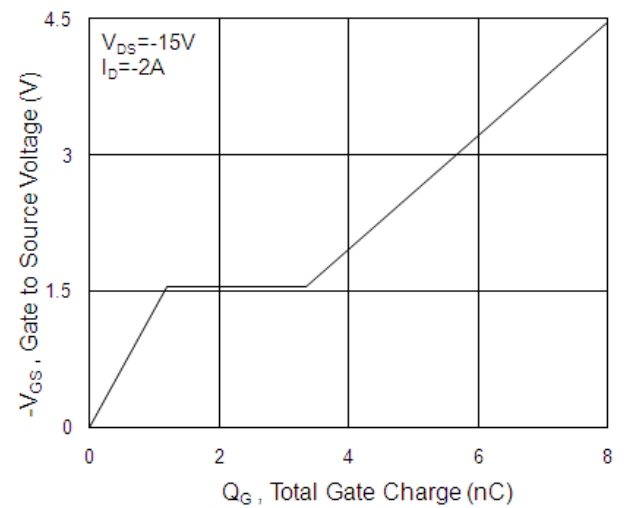
**Fig.1 Typical Output Characteristics**



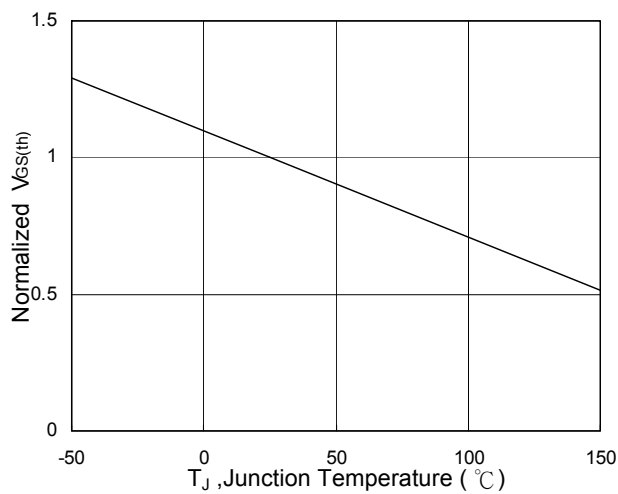
**Fig.2 On-Resistance vs. G-S Voltage**



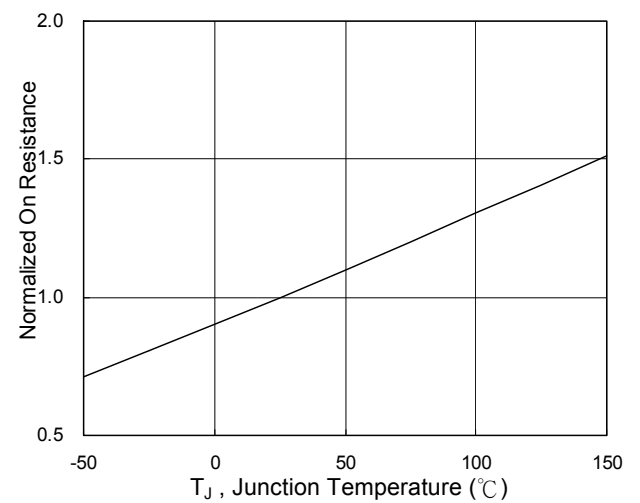
**Fig.3 Forward Characteristics Of Reverse**



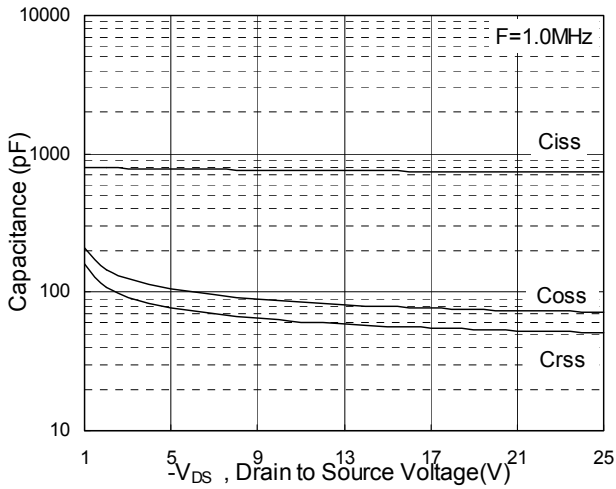
**Fig.4 Gate-Charge Characteristics**



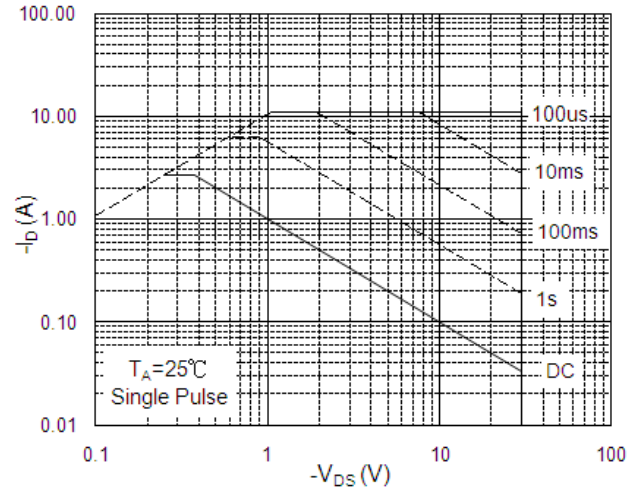
**Fig.5 Normalized V<sub>GS(th)</sub> vs. T<sub>J</sub>**



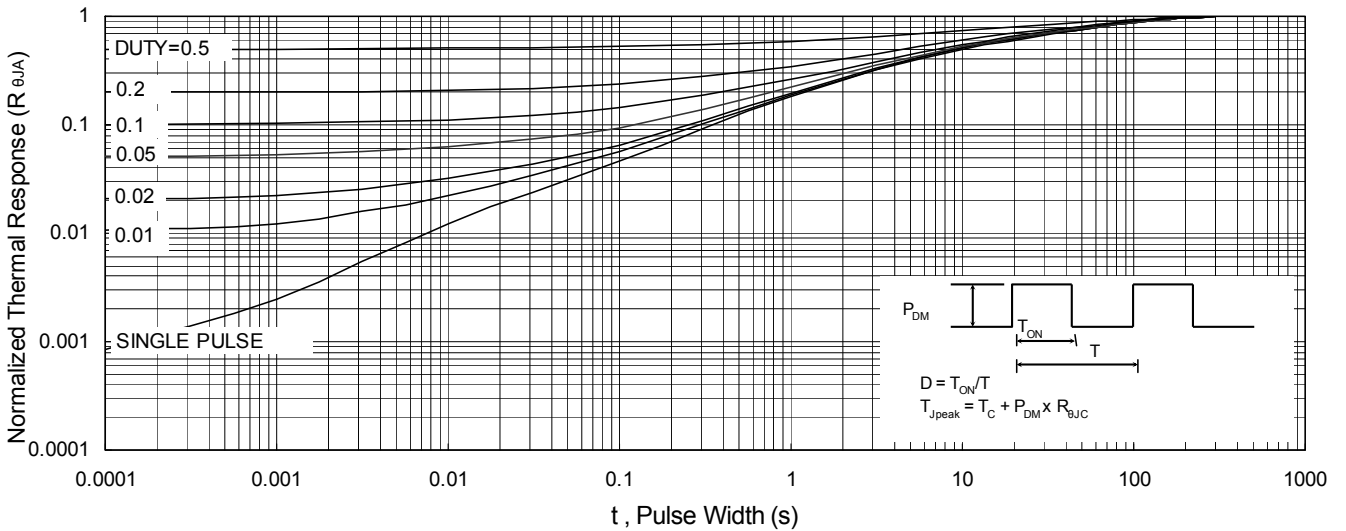
**Fig.6 Normalized R<sub>DS(on)</sub> vs. T<sub>J</sub>**



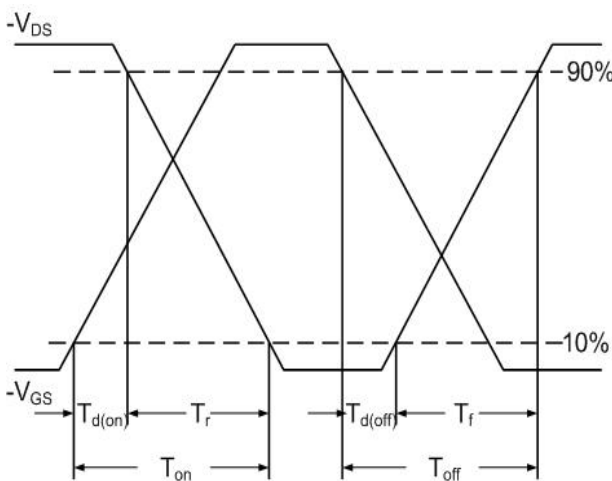
**Fig.7 Capacitance**



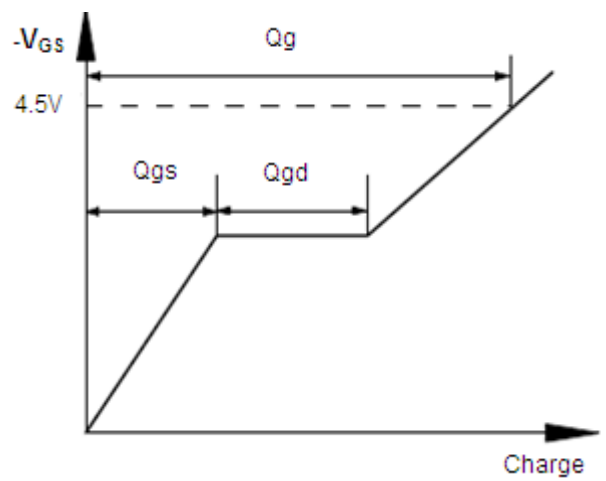
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Gate Charge Waveform**



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