

General Description

The WST3416 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.1V. This device is suitable for use as a load switch or in PWM applications. It is ESD protected.

Features

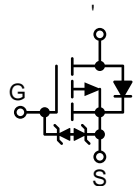
- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent $C_{dv/dt}$ effect decline
- Green Device Available

Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D
20V	18m Ω	6.5A

Applications

- High Frequency Point-of-Load Synchronous
Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

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a


Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 8	V
$I_D@T_c=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	6.5	A
$I_D@T_c=70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5V^1$	5.2	A
I_{DM}	Pulsed Drain Current ²	30	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ³	1.4	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	---	125	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	80	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	20	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.018	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =4.5V, I _D =6.5A	---	18	24	mΩ
		V _{GS} =2.5V, I _D =5.5A	---	22	28	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	0.4	0.7	1.1	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-3.1	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =16V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =16V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±12V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =6.5A	---	50	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.8	3	Ω
Q _g	Total Gate Charge (4.5V)	V _{DS} =15V, V _{GS} =4.5V, I _D =6.5A	---	10	15.0	nC
Q _{gs}	Gate-Source Charge		---	4.2	8.9	
Q _{gd}	Gate-Drain Charge		---	2.6	5.2	
T _{d(on)}	Turn-On Delay Time	V _{DS} =10V, V _{GS} =4.5V, R _G =3Ω RL=1.54Ω	---	280	---	ns
T _r	Rise Time		---	328	---	
T _{d(off)}	Turn-Off Delay Time		---	3.76	---	us
T _f	Fall Time		---	2.24	---	
C _{iss}	Input Capacitance	V _{DS} =10V, V _{GS} =0V, f=1MHz	---	1295	1650	pF
C _{oss}	Output Capacitance		---	160	---	
C _{rss}	Reverse Transfer Capacitance		---	87	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	2.0	A
I _{SM}	Pulsed Source Current ^{2,4}		---	---	10	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.1	V
t _{rr}	Reverse Recovery Time	I _F =6.5A, dI/dt=100A/μs, T _J =25°C	---	31	41	nS
Q _{rr}	Reverse Recovery Charge		---	6.8	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper, t<=10sec.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

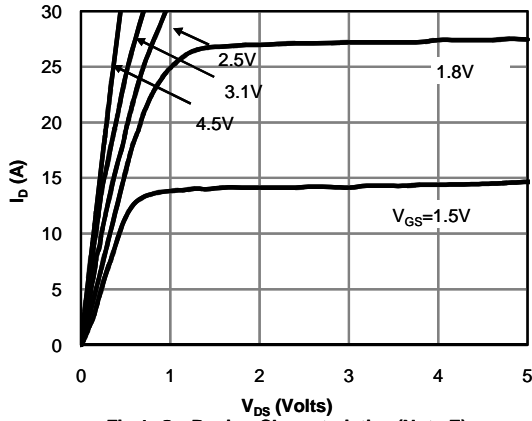


Fig 1: On-Region Characteristics (Note E)

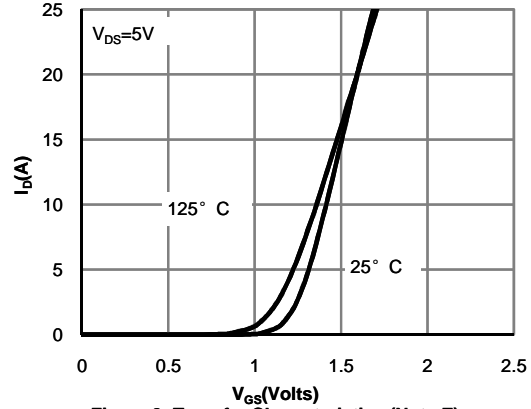


Figure 2: Transfer Characteristics (Note E)

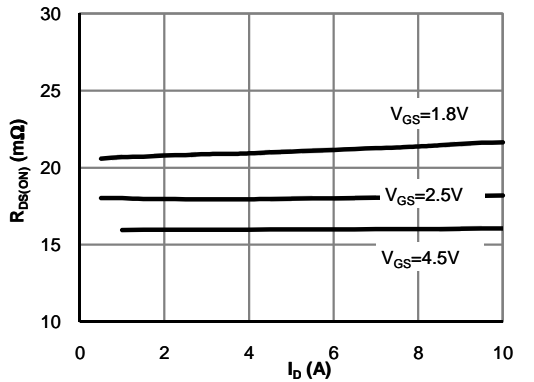


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

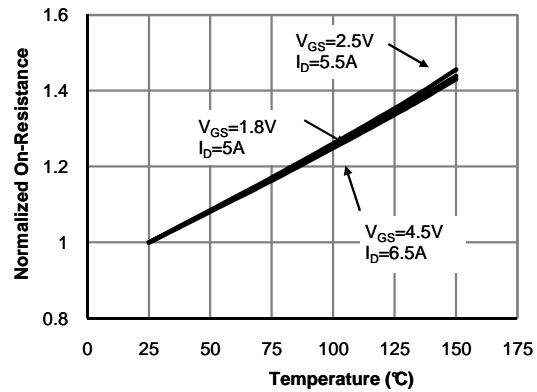


Figure 4: On-Resistance vs. Junction Temperature (Note E)

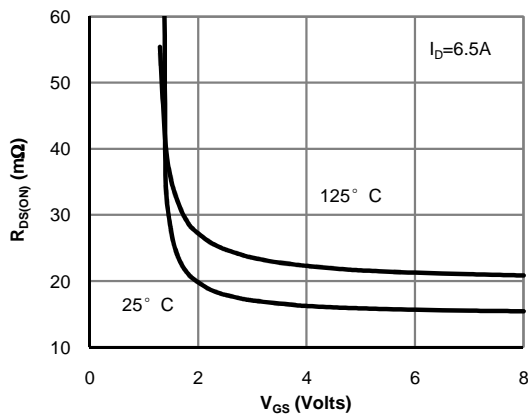


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

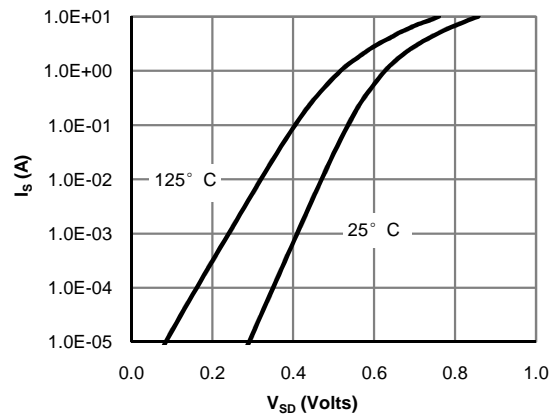


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

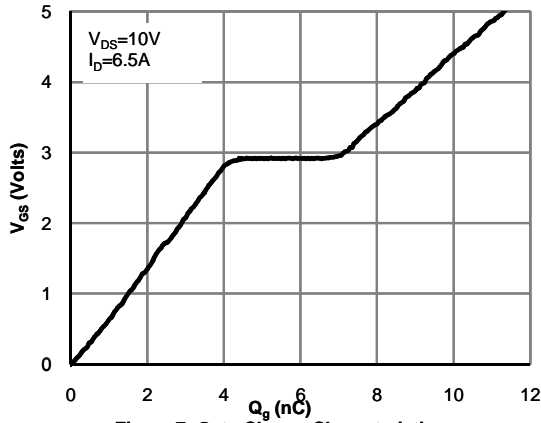


Figure 7: Gate-Charge Characteristics

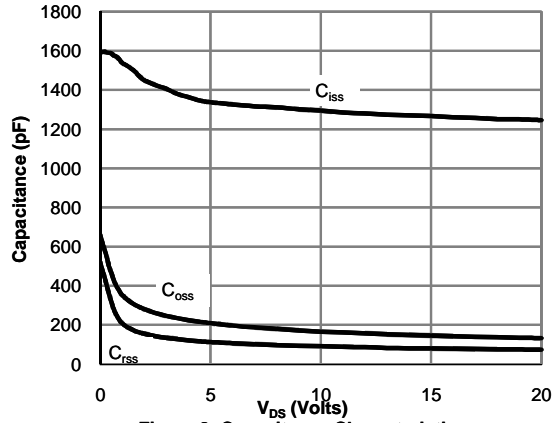


Figure 8: Capacitance Characteristics

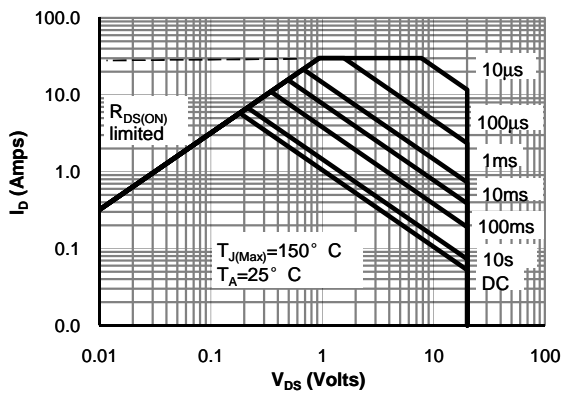


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

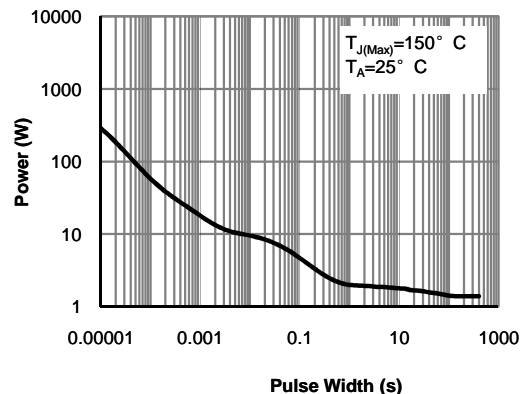


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

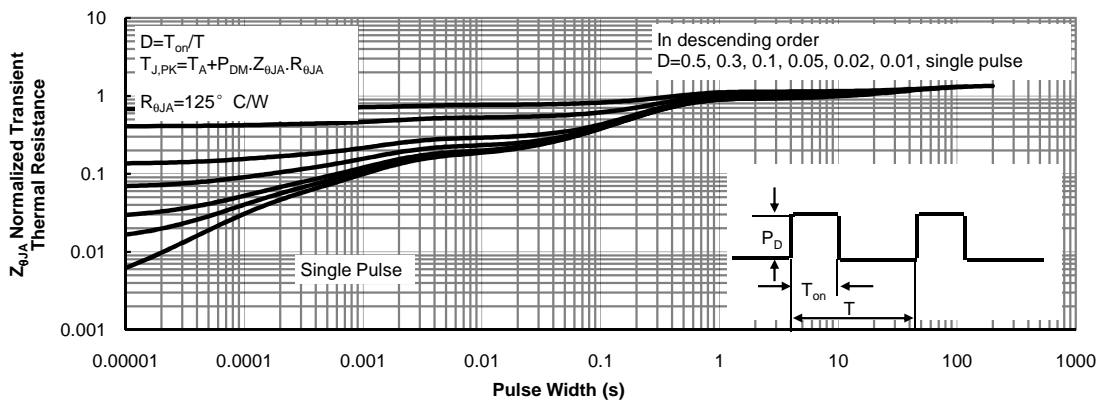


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



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