

General Description

The WSD6075DN56 is the highest performance trench N-Ch and P-Channel MOSFET with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The WSD6075DN56 meet the RoHS and Green Product requirement 100% E_{AS} guaranteed with full function reliability approved.

Features

- 100% UIS + R_g Tested.
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)
- Moisture Sensitivity Level MSL1 (per JEDEC J-STD-020D)

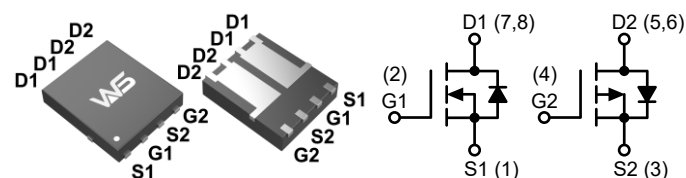
Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D
60V	28m Ω	20A
-60V	58m Ω	-15A

Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems.

DFN5X6-8L Pin Configuration



Absolute Maximum Ratings ($T_A=25^{\circ}\text{C}$, Unless Otherwise Noted)

Symbol	Parameter		Rating		Units
			N-Channel	P-Channel	
V _{DS}	Drain-Source Voltage		60	-60	V
V _{GS}	Gate-Source Voltage		±20	±20	
I _D	Continuous Drain Current	T _C =25°C	20	-15	A
		T _C =100°C	15	-11	
I _{DM} ¹	Pulse Drain Current	T _C =25°C	60	-45	
P _D	Maximum Power Dissipation	T _C =25°C	20.8		W
		T _C =100°C	8.3		
E _{AS} ³	Avalanche Energy, Single pulse	L=0.5mH	16	25	mJ
I _{AS} ³	Avalanche Current, Single pulse	L=0.5mH	8	10	A
T _{STG}	Storage Temperature Range		-55 to 150		°C
T _J	Operating Junction Temperature Range		150		
R _{θJA} ²	Thermal Resistance-Junction to Ambient	Steady State	80		°C/W
R _{θJC}	Thermal Resistance-Junction to Case	Steady State	6.0		

N-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	60	---	---	V
$R_{DS(ON)}^4$	Static Drain-Source On-Resistance	$V_{GS}=10V$, $I_D=7.5A$	---	28	32	m Ω
		$V_{GS}=4.5V$, $I_D=4.5A$	---	35	38	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=250\mu A$	1.0	1.4	2.5	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=48V$, $V_{GS}=0V$	---	---	1.0	μA
		$T_J=85^{\circ}\text{C}$	---	---	30	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
R_G^5	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1.0\text{MHz}$	---	2.8	---	Ω
Q_g^5	Total Gate Charge (4.5V)	$V_{DS}=30V$, $V_{GS}=10V$, $I_D=7A$	---	5.4	---	nC
Q_g^5	Total Gate Charge (10V)		---	11	15	
Q_{gs}^5	Gate-Source Charge		---	2.2	---	
Q_{gd}^5	Gate-Drain Charge		---	2.0	---	
$T_{d(on)}^5$	Turn-On Delay Time	$V_{DD}=30V$, $R_L=30\Omega$, $I_{DS}=1A$, $V_{GEN}=10V$, $R_G=6\Omega$	---	10	18	ns
T_r^5	Rise Time		---	6	11	
$T_{d(off)}^5$	Turn-Off Delay Time		---	21	38	
T_f^5	Fall Time		---	5.3	10	
C_{iss}^5	Input Capacitance	$V_{DS}=30V$, $V_{GS}=0V$, $f=1.0\text{MHz}$	---	555	720	pF
C_{oss}^5	Output Capacitance		---	61	---	
C_{rss}^5	Reverse Transfer Capacitance		---	32	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current	$T_C=25^{\circ}\text{C}$	---	---	20	A
V_{SD}^4	Diode Forward Voltage	$V_{GS}=0V$, $I_{SD}=4A$	---	0.8	1.1	V
t_{rr}	Reverse Recovery Time	$I_{SD}=7A$, $di_{SD}/dt=100A/\mu s$	---	21	---	ns
Q_{rr}	Reverse Recovery Charge		---	20	---	nC

Note:

1. Pulse width limited by maximum junction temperature.
2. Surface mounted on 1in² pad area.
3. UIS tested and pulse width limited by maximum junction temperature (initial temperature $T_J=25^{\circ}\text{C}$).
4. Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. Guaranteed by design, not subject to production testing.

P-Channel Electrical Characteristics ($T_J=25^{\circ}\text{C}$, Unless Otherwise Noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V$, $I_D=-250\mu A$	-60	---	---	V
$R_{DS(ON)}^4$	Static Drain-Source On-Resistance	$V_{GS}=-10V$, $I_D=-7A$	---	58	65	m Ω
		$V_{GS}=-4.5V$, $I_D=-4A$	---	75	83	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}$, $I_D=-250\mu A$	-1.0	-1.9	-3.0	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-48V$, $V_{GS}=0V$	---	---	-1.0	μA
		$T_J=85^{\circ}\text{C}$	---	---	-30	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V$, $V_{DS}=0V$	---	---	± 100	nA
R_G^5	Gate Resistance	$V_{DS}=0V$, $V_{GS}=0V$, $f=1.0\text{MHz}$	---	10.0	---	Ω
Q_g^5	Total Gate Charge (-4.5V)	$V_{DS}=-30V$, $V_{GS}=-10V$, $I_D=-7A$	---	5.5	---	nC
Q_g^5	Total Gate Charge (-10V)		---	11.5	15.5	
Q_{gs}^5	Gate-Source Charge		---	2.3	---	
Q_{gd}^5	Gate-Drain Charge		---	4.3	---	
$T_{d(on)}^5$	Turn-On Delay Time	$V_{DD}=-30V$, $R_L=30\Omega$, $I_{DS}=-1A$, $V_{GEN}=-10V$, $R_G=6\Omega$	---	9	15	ns
T_r^5	Rise Time		---	5	10	
$T_{d(off)}^5$	Turn-Off Delay Time		---	40	72	
T_f^5	Fall Time		---	27	40	
C_{iss}^5	Input Capacitance	$V_{DS}=-30V$, $V_{GS}=0V$, $f=1.0\text{MHz}$	---	530	700	pF
C_{oss}^5	Output Capacitance		---	65	---	
C_{rss}^5	Reverse Transfer Capacitance		---	35	---	

Diode Characteristics

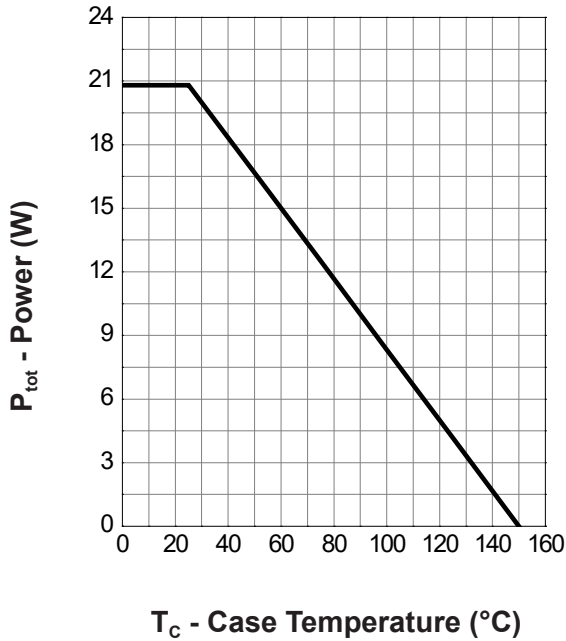
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Current	$T_C=25^{\circ}\text{C}$	---	---	-15	A
V_{SD}^4	Diode Forward Voltage	$V_{GS}=0V$, $I_{SD}=-4A$	---	-0.8	-1.1	V
t_{rr}	Reverse Recovery Time	$I_{SD}=-7A$, $di_{SD}/dt=100A/\mu s$	---	27	---	ns
Q_{rr}	Reverse Recovery Charge		---	32	---	nC

Note:

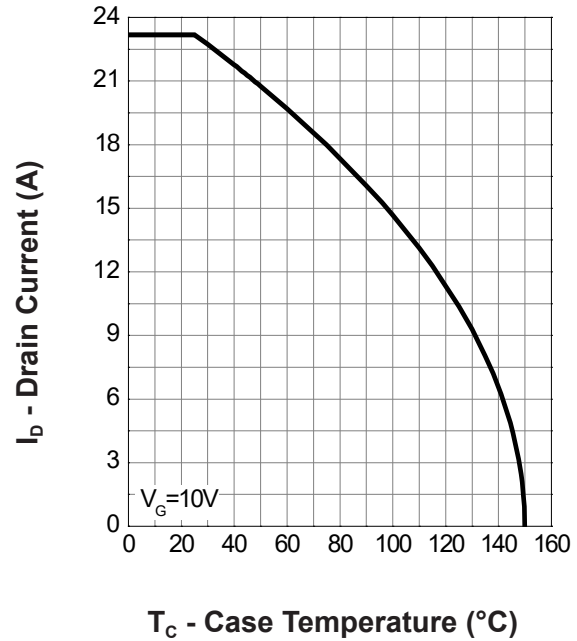
1. Pulse width limited by maximum junction temperature.
2. Surface mounted on 1in² pad area.
3. UIS tested and pulse width limited by maximum junction temperature (initial temperature $T_J=25^{\circ}\text{C}$).
4. Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics

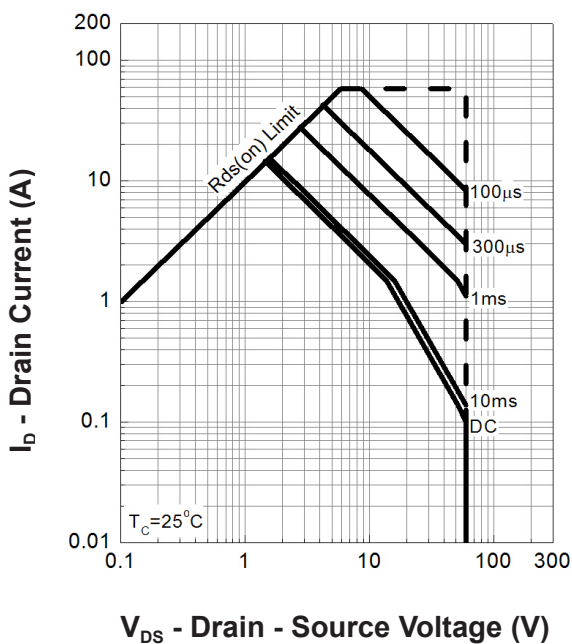
Power Dissipation



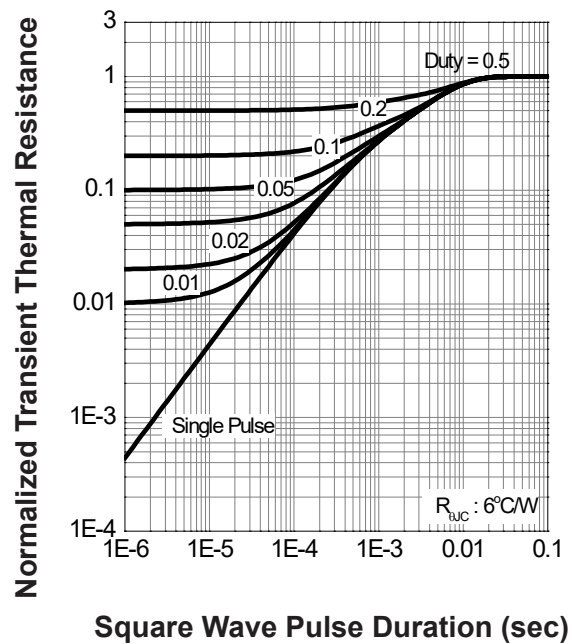
Drain Current



Safe Operation Area

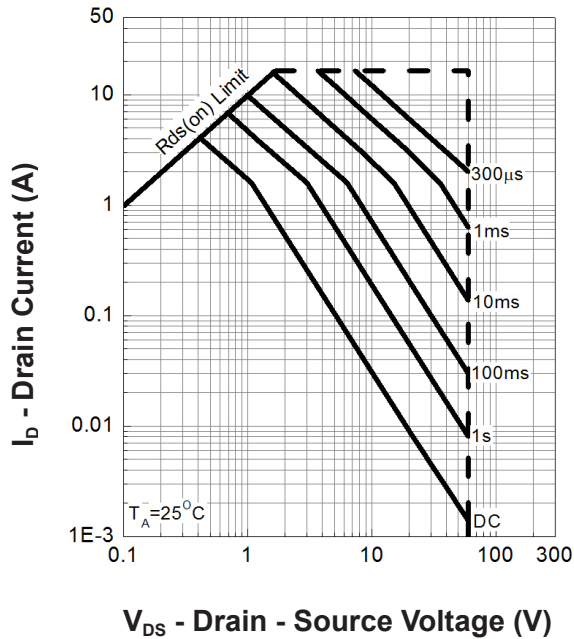


Thermal Transient Impedance

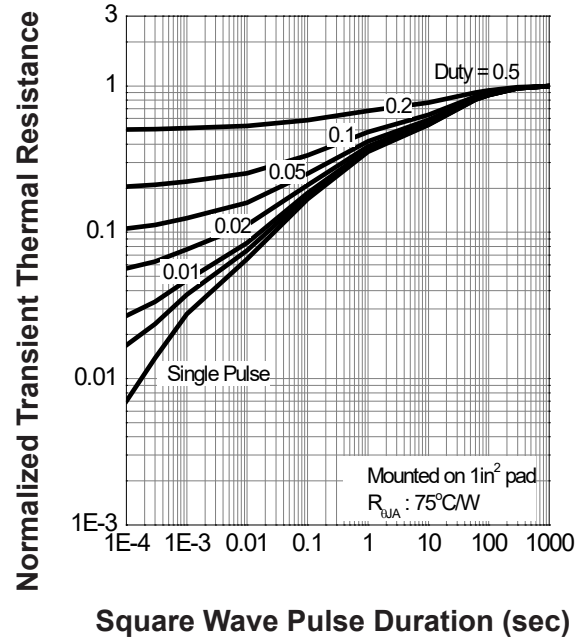


N-Channel Typical Characteristics (Cont.)

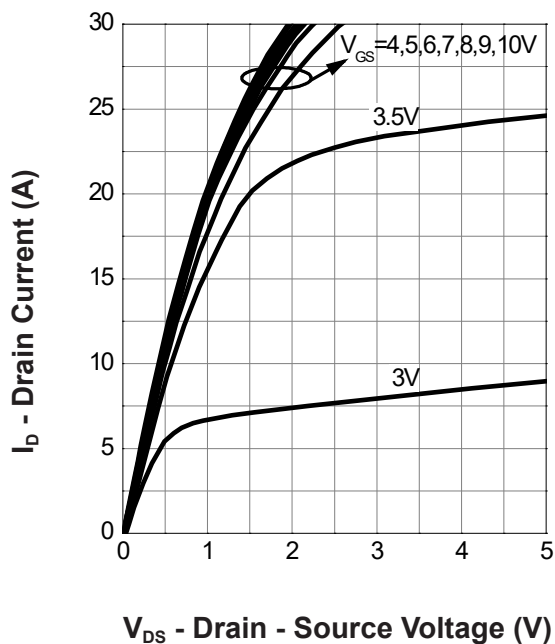
Safe Operation Area



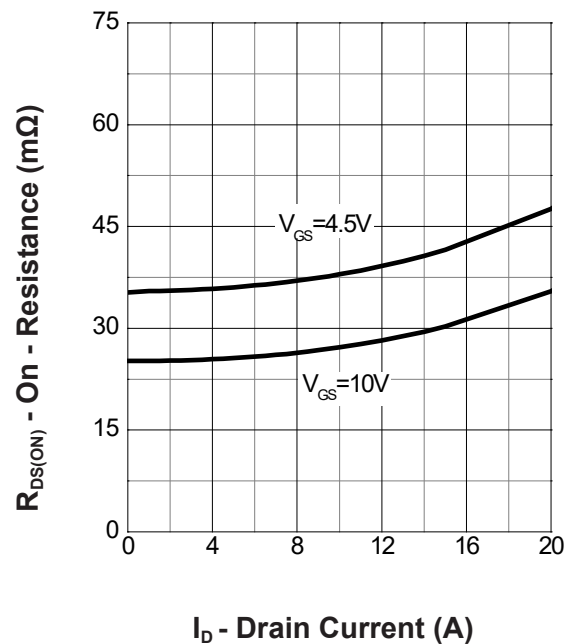
Thermal Transient Impedance



Output Characteristics

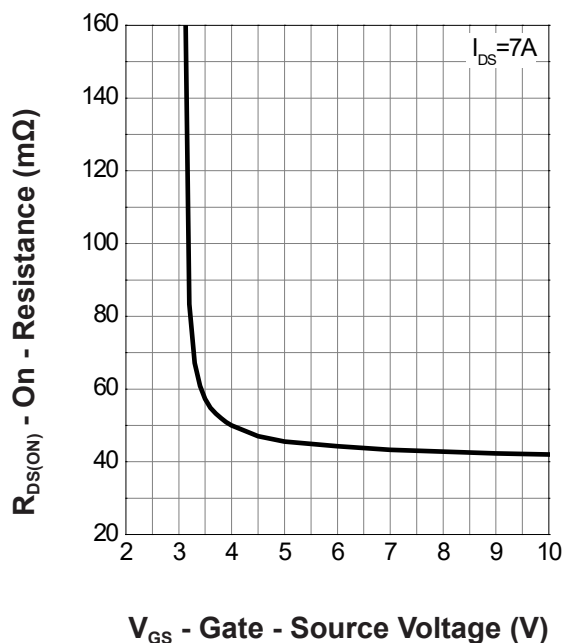


Drain-Source On Resistance

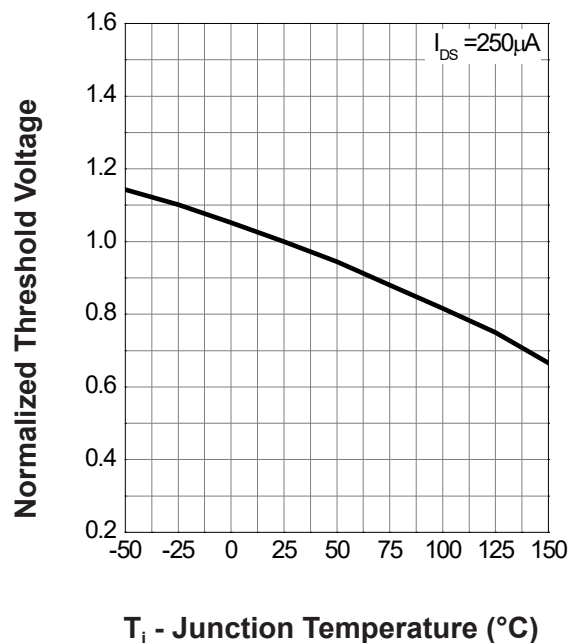


N-Channel Typical Characteristics (Cont.)

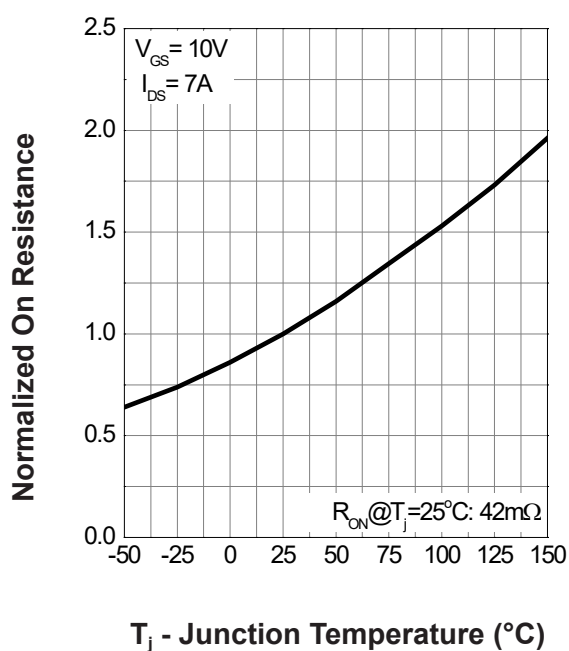
Gate-Source On Resistance



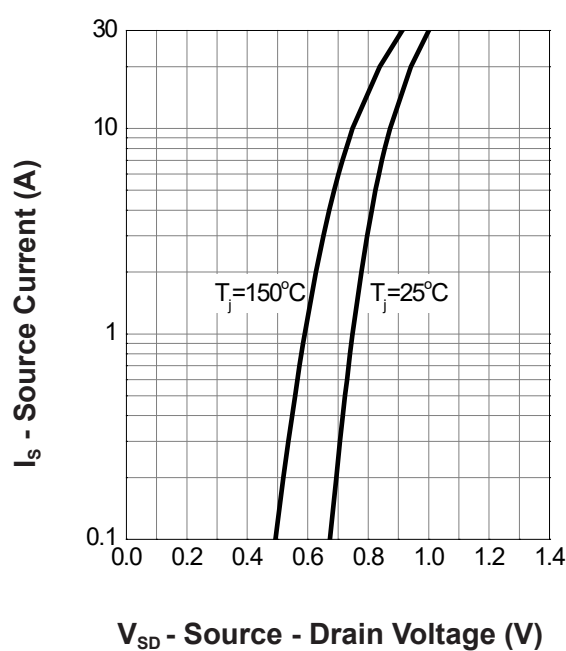
Gate Threshold Voltage



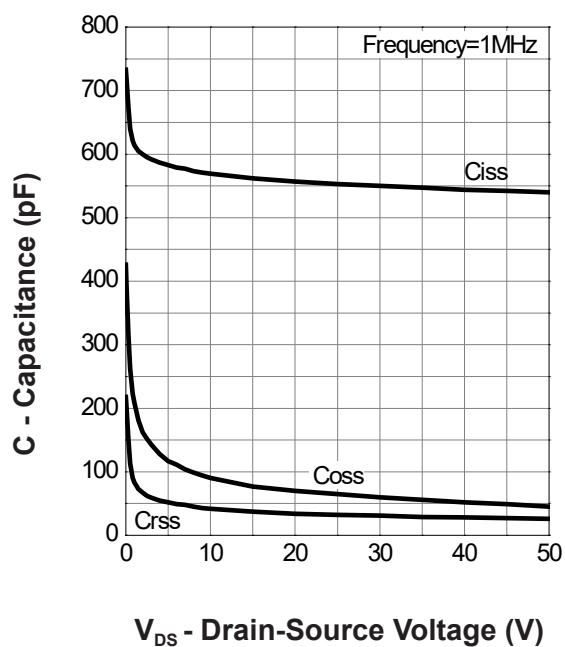
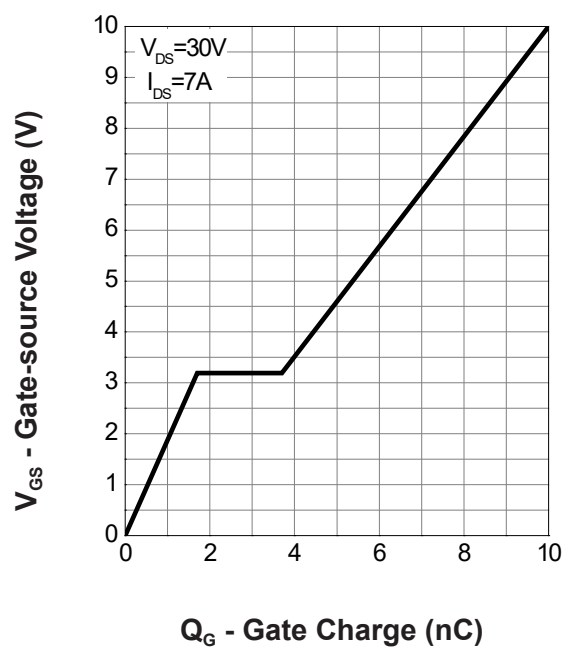
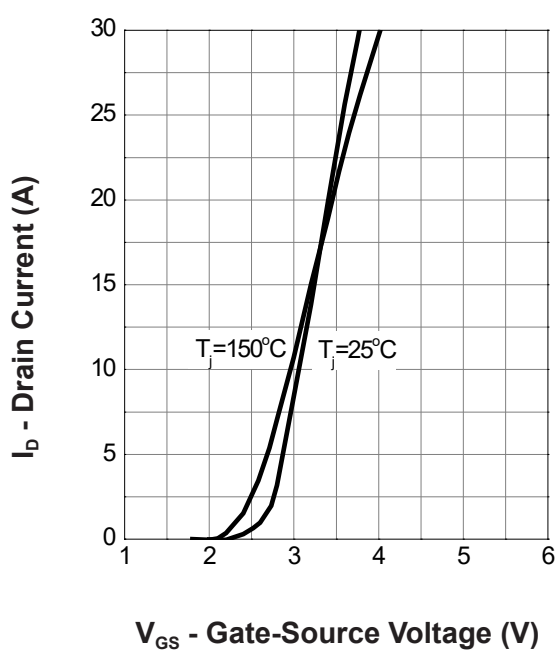
Drain-Source On Resistance



Source-Drain Diode Forward

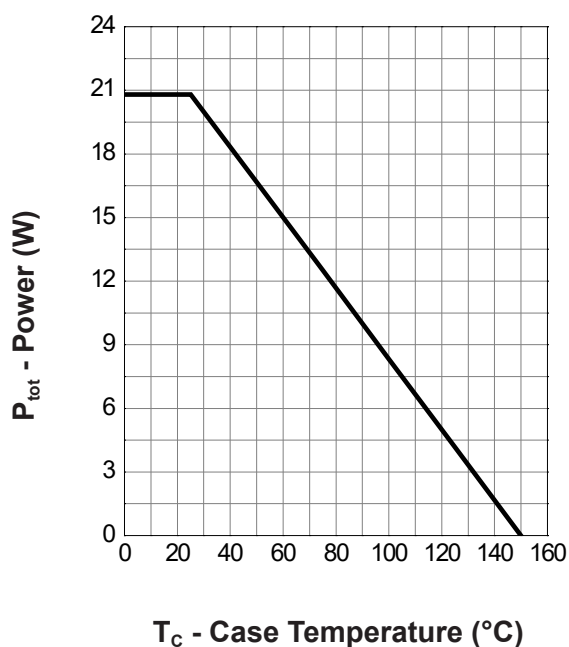


N-Channel Typical Characteristics (Cont.)

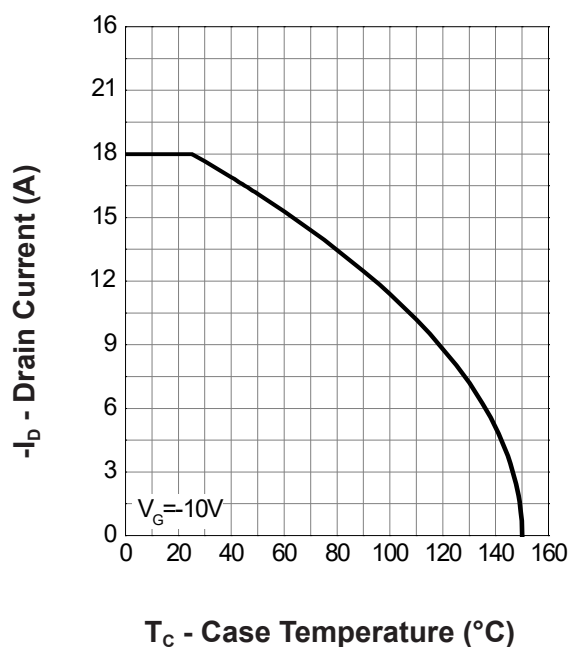
Capacitance

Gate Charge

Transfer Characteristics


P-Channel Typical Characteristics

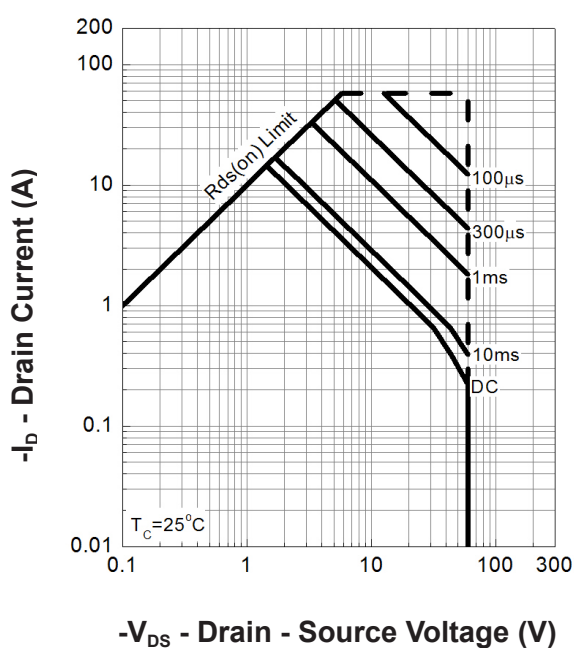
Power Dissipation



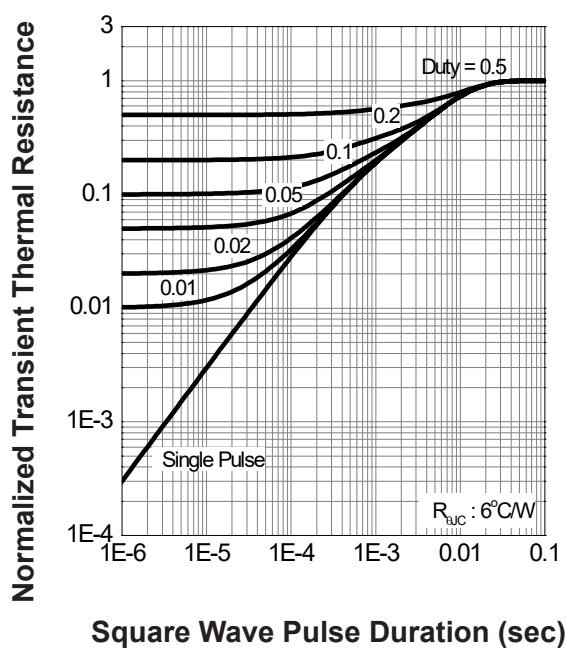
Drain Current



Safe Operation Area

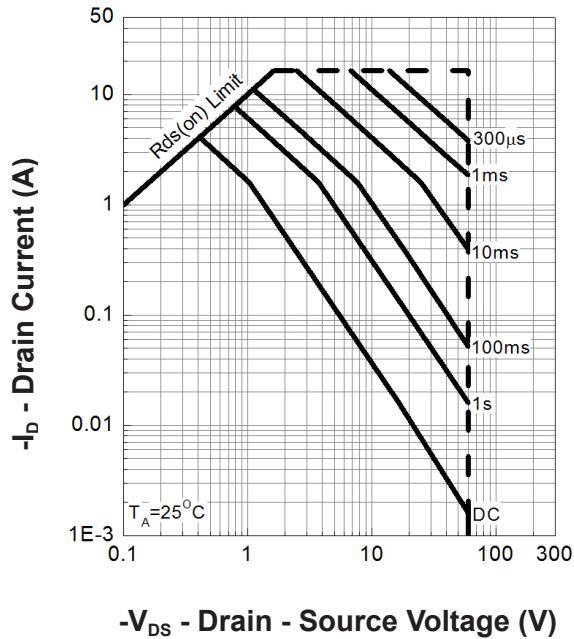


Thermal Transient Impedance

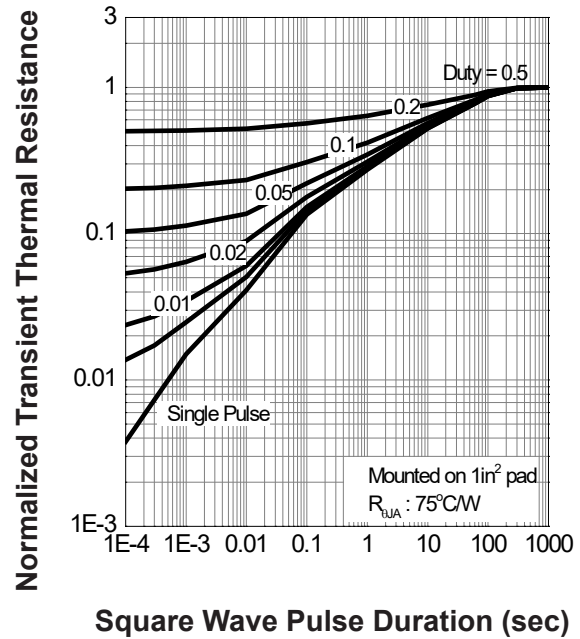


P-Channel Typical Characteristics (Cont.)

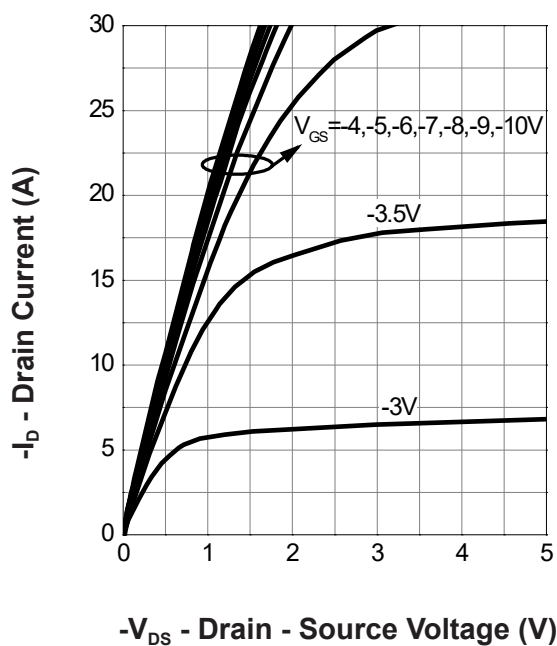
Safe Operation Area



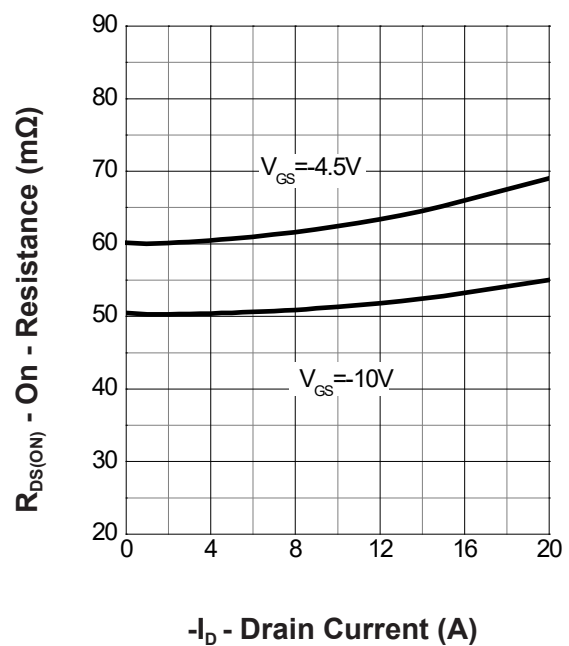
Thermal Transient Impedance



Output Characteristics

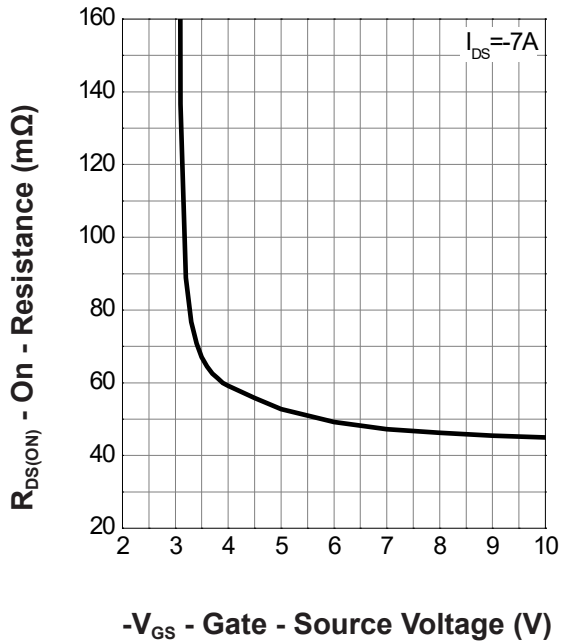


Drain-Source On Resistance

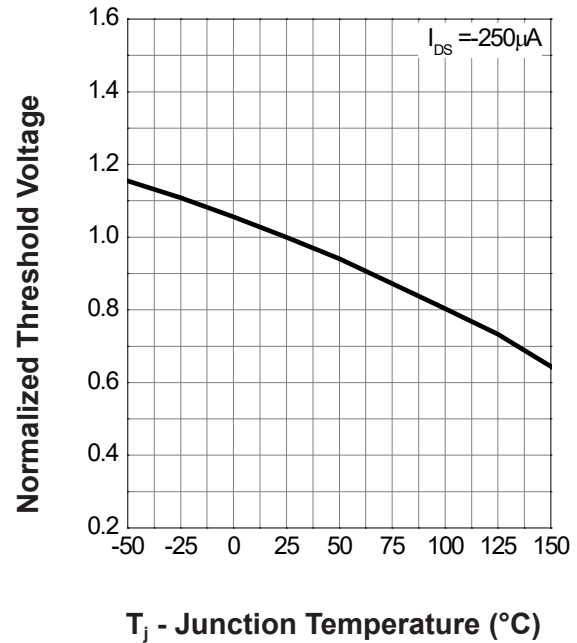


P-Channel Typical Characteristics (Cont.)

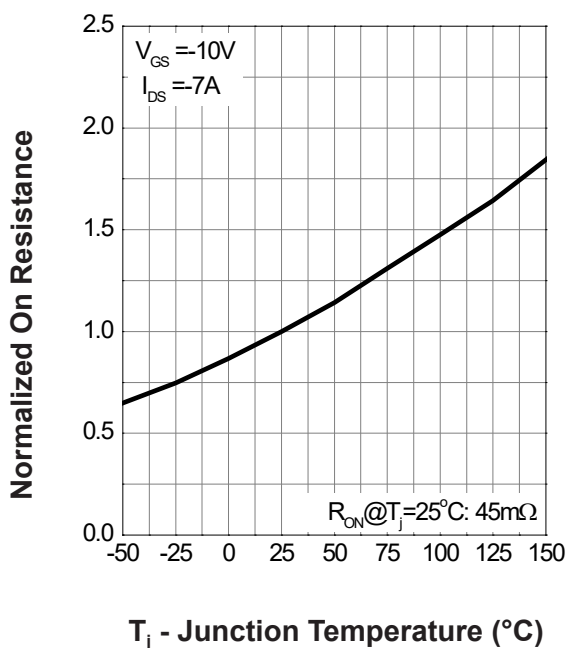
Gate-Source On Resistance



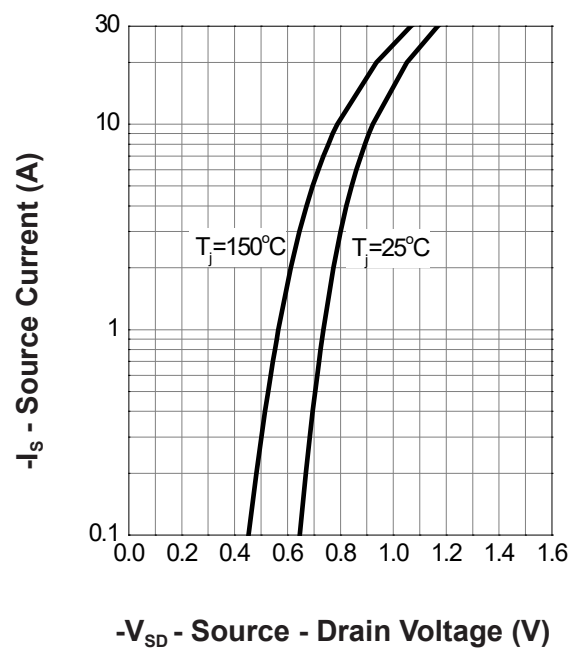
Gate Threshold Voltage



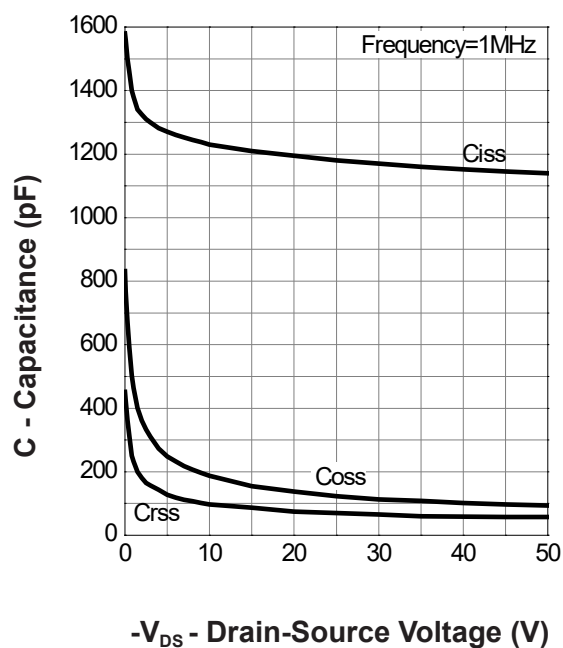
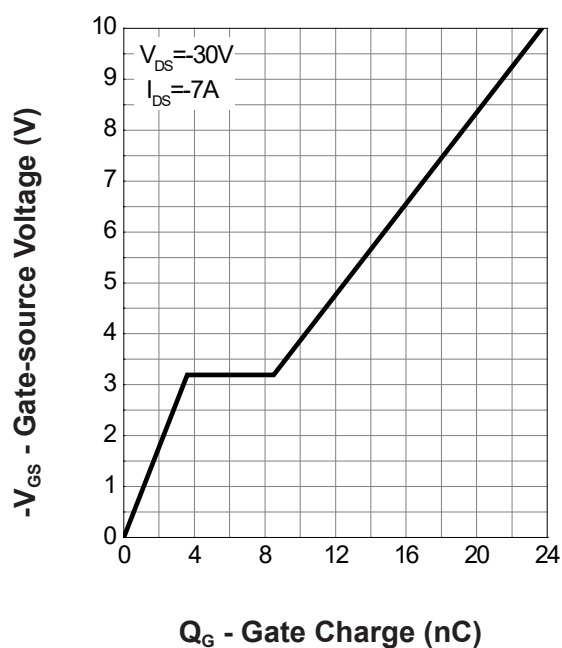
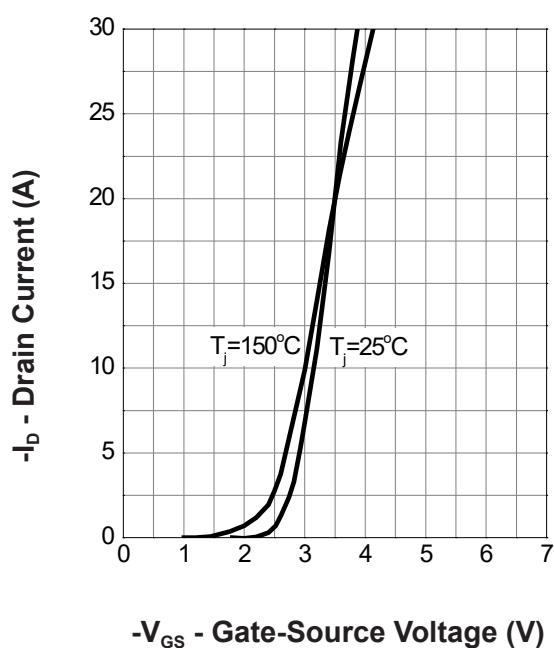
Drain-Source On Resistance



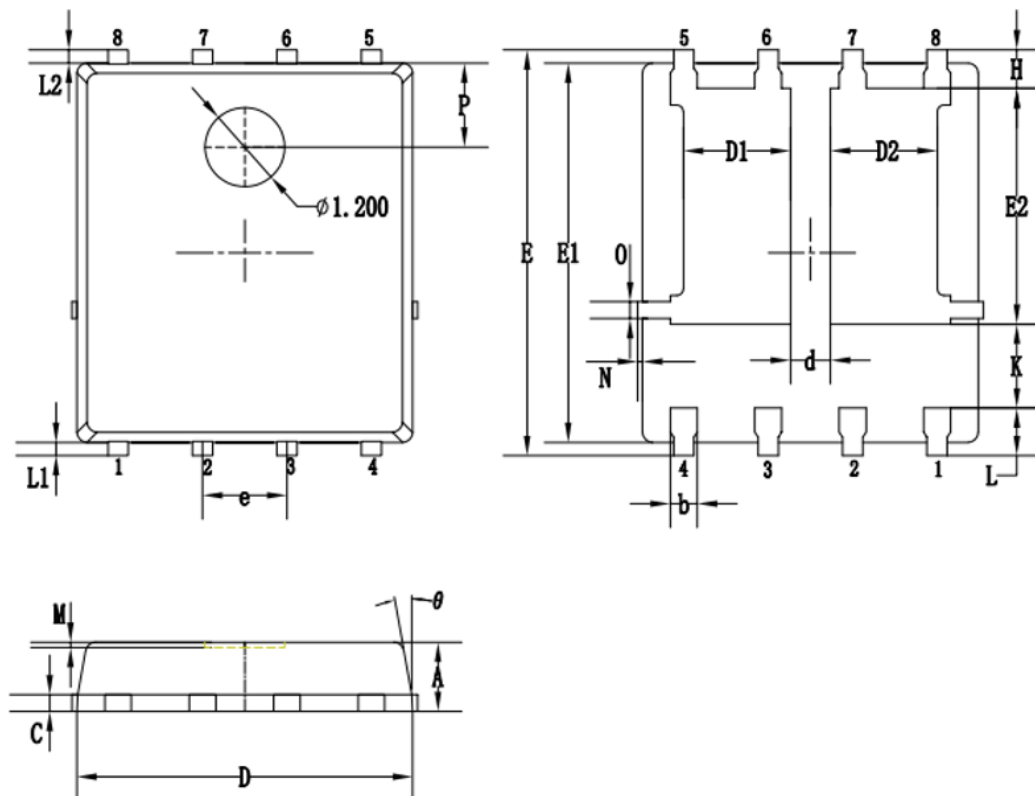
Source-Drain Diode Forward



P-Channel Typical Characteristics (Cont.)

Capacitance

Gate Charge

Transfer Characteristics


Packaging information



SYMBOLS	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.05	1.20
b	0.35	0.40	0.50
C	0.20	0.25	0.35
D	4.90	5.05	5.20
D1/D2	1.51	1.61	1.71
d	0.50	0.60	0.70
E	6.00	6.15	6.30
E1	5.60	5.75	5.90
E2	3.47	3.57	3.67
e	1.27 BSC.		
H	0.48	0.58	0.68
K	1.17	1.27	1.37
L	0.64	0.74	0.84
L1/L2	0.20 REF.		
θ	8°	10°	12°
M	0.08 REF.		
N	0	-	0.15
O	0.25 REF.		
P	1.28 REF.		

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